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Intel(R) Firmware Support Package (Intel® FSP) for Intel® Braswell Platform -

Release Notes

Release Version: 01010401

November 16, 2015

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RELEASE NOTES CONTENTS

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1. OVERVIEW

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This package contains required binary image(s) and collateral for the

Intel(R) Firmware Support Package (Intel® FSP) for Intel® Braswell platform.

It supports platforms with Braswell SOC.

This FSP binary has been validated on a Cherry Hill CRB.

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2. RELEASE INFORMATION

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- Compliant with FSP 1.1 External Architecture Specification.

This release package contains

1. FSP Binary
2. Boot Setting File (BSF)
3. Integration Guide
4. Release Notes

5. FSP Sample Code

6. Graphics Video BIOS Table (VBT) Files

7. Graphics VBT BSF File

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3. INTEGRATION NOTES

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The FSP can be integrated with any bootloader of choice and the integration requirements are documented in the Integration Guide released in this package.

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4. SUPPORTED FEATURES

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- Braswell C0 & D1 stepping SOC
- MRC Version 0x00330007
- MTRR Initialization on all CPU threads
- Graphics Initialization
- SOC IO Controllers Initialization
- PCI Express Root Port Initialization
- Configuration options through Intel binary configuration tool
- Rebase to a different base address through Intel binary configuration tool

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5. FSP CONFIGURATION

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When integrating with a bootloader the FSP should be placed at the same base address that it is configured to.

The default base address for the FSP is documented in the FSP Integration Guide.

The base address for the FSP can be configured to a different address using Intel binary configuration tool.

The FSP also provides a set of configuration options for initializing the SOC and can be customized through Intel binary configuration tool.

Secure Boot can be Enabled/Disabled under the 'Enable Secure Boot' field of the binary configuration tool.
- The 'Auto' selection is deprecated and will be removed in the next release.

Please use Intel binary configuration version 3.2 or newer with this release of FSP.

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6. GRAPHICS CONFIGURATION

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Graphics initialization is supported in this release of FSP. When integrating with a bootloader a reference to the VBT should be passed in to FSP via the UPD PcdGraphicsConfigPtr field.

Preconfigured graphics VBT files for use with the Braswell RVP and the Cherryview CRB platform are included in this release. Additional configuration of the VBT graphics files are possible via the Intel® BMP utility using the VBT BSF, contact your Intel representative for access to BMP.

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7. LIMITATIONS

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8. KNOWN ISSUES

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When using BCT to configure "Pnp-Power Performance" option it displays as
blank, enable, and disable. Leaving this field blank will leave as default
value of 0x3. The settings for this field can be overwritten in Coreboot by
modifying UPD PcdPnpSettings field in romstage_fsp_rt_buffer_callback in Coreboot
with the following alternative options:

0x0 , " Disable"

0x1 , " Power"

0x2 , " Performance"

0x3 , " Power & Performance" - Default

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9. CHANGE LOG

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Release 01010401 FSP_IMAGE_ID BSWSBFSP:

- Secure Boot capability added
- Support for IOTG Android OS Boot added
- DDR3 AutoSelfRefresh PCD was added
- Windows 10 Boot Validated
- Bug Fixes
    - LPSS Device Initialization was fixed

Release 01010200:

- Bug Fixes
    - Address Win 8.1 Yellow Bangs
    - Resolve Win 7 boot when CMOS cleared

- Resolve Win 8.1 LPSS Yellow Bang
- Enable Turbo mode support
- Resolve AzaliaVerbTable issue pre-OS

Release 01000200:

- Graphics Updates
- Bug Fixes

Release 01000001:

- Pre Boot Graphics
- Fast Boot
- S3

Release 00070001:

- Initial FSP release