Device Bay Design Guide

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11/4/98

Draft

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Preface

Device Bay is a new form factor standard proposed by the Device Bay Promoters – Compaq, Microsoft and Intel. Device Bay leverages off two emerging industry standard serial interfaces – USB and IEEE1394. For the users, Device Bay enables ease-of-use, modular expansion and security, among other benefits. For the manufacturers, Device Bay enables architectural flexibility. Device Bay can be implemented in many applications such as desktop/laptop PCs, workstation, servers, consumer electronics, test/measurement, data acquisition, industrial controls, medical, etc.

Device Bay Interface Specification defines three device form factors with all necessary electrical, mechanical and software interfaces. The specification defines enough interface information for interoperability, at the same time leave rooms for cost/performance trade-off, product differentiation, innovation and to support various applications. Several system and device prototypes have been built and tested by Compaq and many of the Device Bay Adopters – manufacturers of Device Bay devices, ICs and connectors/cables – to proof the specification robustness. The specification has been fine-tuned whenever appropriate, based on the lessons learned from the prototypes.

This document contains information for the implementers to avoid pit-falls that we have gone through during several rounds of prototypes, and to enable building blocks for the industry to adopt Device Bay in a relatively short time period. Several example implementations are illustrated in this document, which can be used as guidelines. These example implementations may be modified for a specific application or product, provided that necessary interfaces comply with the Device Bay Interface Specification. These examples are to illustrate flexibility of the specification and occasionally to show how various types of parts can be implemented. The connectors illustrated in this document are proposed to be reference design parts and some of them may eventually become de facto standards. The proposed connectors and cable assemblies need to be reviewed by the purchasers and manufacturers of these parts to ensure that they will meet all the functional and appropriate regulation requirements. The vendor listing in this document is for information purposes only and it should not be viewed as *Promoters'* endorsement. Each vendor of Device Bay parts, devices or systems should do necessary diligence on all product/service aspects such as market viability, product functionality, performance, safety and cost.

This document is a living document, and currently is available via the Device Bay web site (http://www.device-bay.org/). All questions and comments are to be communicated via Device Bay Chat line (see the web site for details).

The computer industry has come a long way since a few decades ago. Industry standards have been the breeding ground for today's computers and related hardware and software components. Manufacturers and users alike have learned to advance the technology and application fronts, respectively, while "older" industry standards are replaced by new ones. Device Bay overcomes many of the shortcomings of existing industry standards, such as IDE and SCSI. The Device Bay proponents would like to think that Device Bay is the wave that will carry many industries into the next millennium.

On behalf of the Device Bay Committee, we would like to thank all the individuals from the *Adopters* companies for their efforts in developing the Device Bay Interface Specification, manufacturing sample parts/devices, and working out issues on the Device Bay system/device prototypes and software.

Kevin Leigh & Jeff Wolford (Editors)
Compaq Computer Corporation

Contents

1. Introduction

In this document we will refer to the Device Bay Interface Specification [1] as "the DB spec." Device Bay *promoters* and *adopters* have spent a significant amount of resources in developing the specification to ensure interoperability of Device Bay (DB) hardware and software components. The DB spec. describes detail requirements on interface buses, power, connector mating area, device mechanical form factors, controller and software. DB can be implemented for portable PCs, desktop PCs, servers, workstation, consumer products, etc. The DB spec. was designed to cover a wide range of applications for different performance and price points. More information on DB and the DB spec. can be found on the DB web site at http://www.device-bay.org/ .

1.1. Purpose

The purpose of this document is to provide implementation examples and tips to help designers implement DB related components, parts, devices and systems. Information in this document is to provide the designers with a starting point for their design. It is NOT meant to replace the engineering that must be done to have a complete compliant and functioning system design. This document is intended to augment the DB spec.

When device form-factor matters, all examples in this document are primarily intended for the DB32 form factor. However, much of the guideline information can be either applied directly to or extrapolated for the DB13 and DB20 form factors. Certain implementations in this document may be suggested as a de facto standard proposal. However, currently there is no standardization body for DB to formally promote and process the adoption of the proposals. In other words, let the market decides on which proposals will be actually adopted.

1.2. References

[1] "Device Bay Interface Specification," Compaq, Microsoft and Intel, 1998.
[2] "USB Specification,"
[3] "1394-1995 High Performance Serial Bus Specification," 1995.
[4] "1394b High Performance Serial Bus Specification," 1998.
[5] "Device Bay High-Speed Interconnectivity Performance Analysis," K.B. Leigh, 1998. [To be released]
[6] "Device Bay Contact List," 1998. [To be released]

1.3. Feedback

Questions and suggestions for this document should be posted on the Device Bay Chat line (see the DB web site for more information).

1.4. Acknowledgement

On behalf of the Device Bay Promoters and Adopters, we would like to thank the following connector vendors[1] for their contributions:

- Molex provided several system interconnect and connector drawings for the example implementations illustrated in this document. Foxconn also provided connector drawings.
- Molex, Foxconn and AMP provided connector and cable assembly samples which we used them in system prototyping.
- Molex, Foxconn, AMP and Berg contributed in defining the reference design connectors.

The above connector vendors contact information is listed in [6], and also on the DB web site.

In the process of creating these samples and system prototypes we have learned several lessons, some of which had helped refine the DB spec. as well as the creation of this document.

[1] Molex, Foxconn, AMP and Berg have been the key players in the Device Bay Connector Workgroup. This workgroup also consisted of other contributors from several storage vendors, 1394 PHY vendors, system OEMs and Microsoft. The members of this workgroup were responsible in defining the Device Bay Connector Requirements (Section 4) of the DB spec.

2. Topologies

Device Bay can be implemented to have different topologies –

- For "local bays," the bays are within the same enclosure as the host.
- For "remote bays," the bays are in a separate enclosure from the host.

DB devices can also be used in systems where there are no DB bays, e.g., a DB device can be semi-permanently mounted (similar to how IDE and SCSI devices are mounted) inside an enclosure [Figure 1(c)], instead of being a "removable" device [Figure 1(a) & (b)]. Let's call this topology to be "internal device." An internal device does not need to be one of DB device form factors.

This section illustrates implementation examples for different DB topologies for generic "PC" systems. For each example DB specific connectors and cable assemblies are highlighted. Whenever appropriate, detail information such as part dimensions and PCB footprints are provided. More detail information, such as DB connectors and cable assemblies are illustrated in Section 3 of this document. Manufacturers of and contacts for the parts shown in this section are listed in [6].

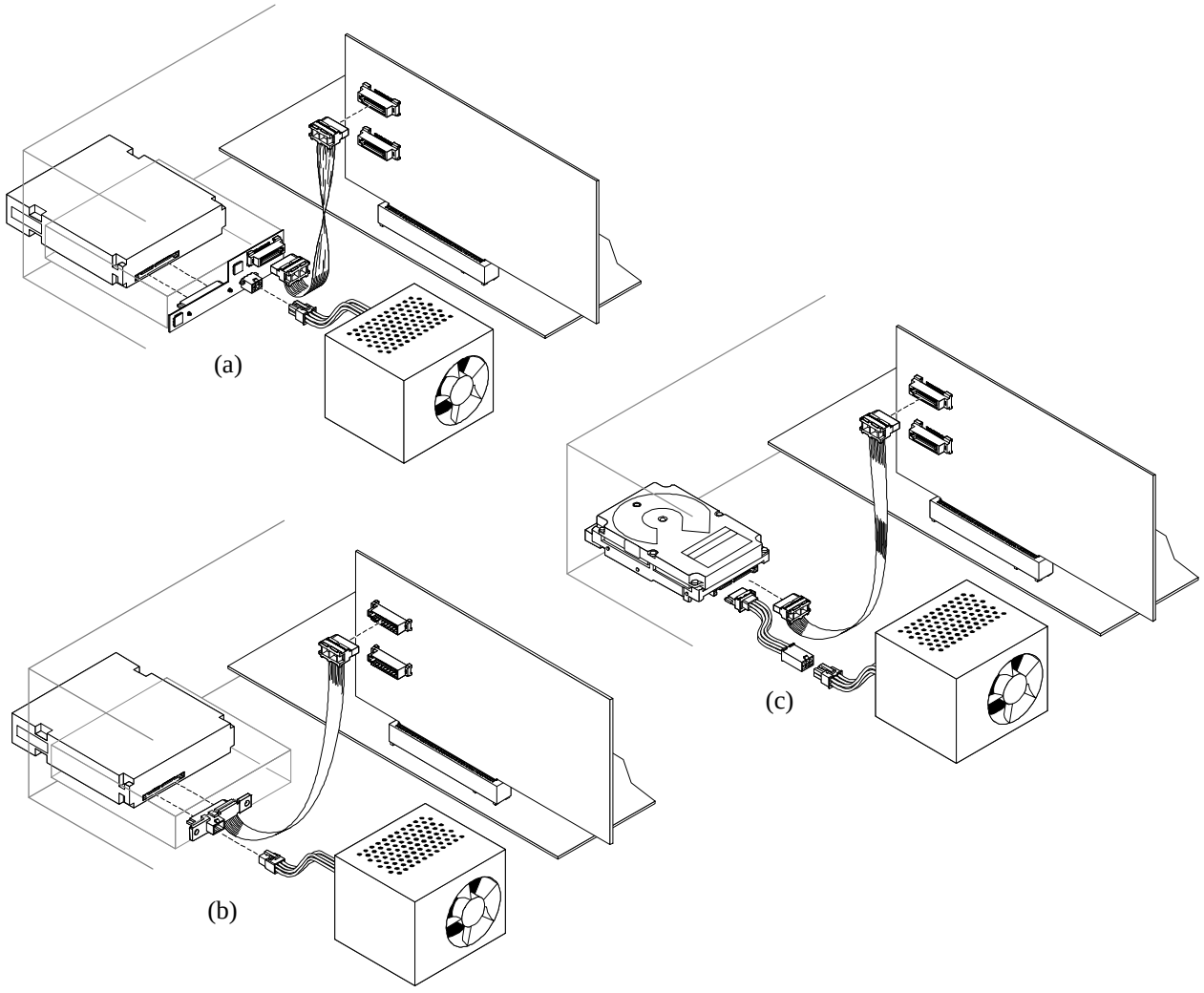


Figure 1. Device Bay device application examples.

2.1. Local Bays

For local bay implementations, the DB (USB and 1394) signals can be from the motherboard, the riser card (Figure 1), or an add-in card. The Device Bay Controller (DBC) can be either ACPI-based or USB-based (see [1] for more details on DBC types). The power can come directly from the host power supply or indirectly from a PCB, such as the motherboard.

Each bay receptacle can be of a PCB- or cable-mount type, depending on several factors such as, power voltage availability, power control, signal data rate, bay configuration choices, etc. Figure 1 (a) and (b) shows a PCB-mount and a cable-mount receptacles, respectively.

Figure 2 shows an example implementation of two vertically-stacked local bays (rear view) using a cable-terminated bay receptacles, power connection directly from the host power supply and the DB signals from a PCB. A legacy (e.g., IDE or SCSI) device and its connectivity are shown here to illustrate that DB devices can coexist with legacy devices. More information on the connectors and cable assemblies are in the later chapters of this document.

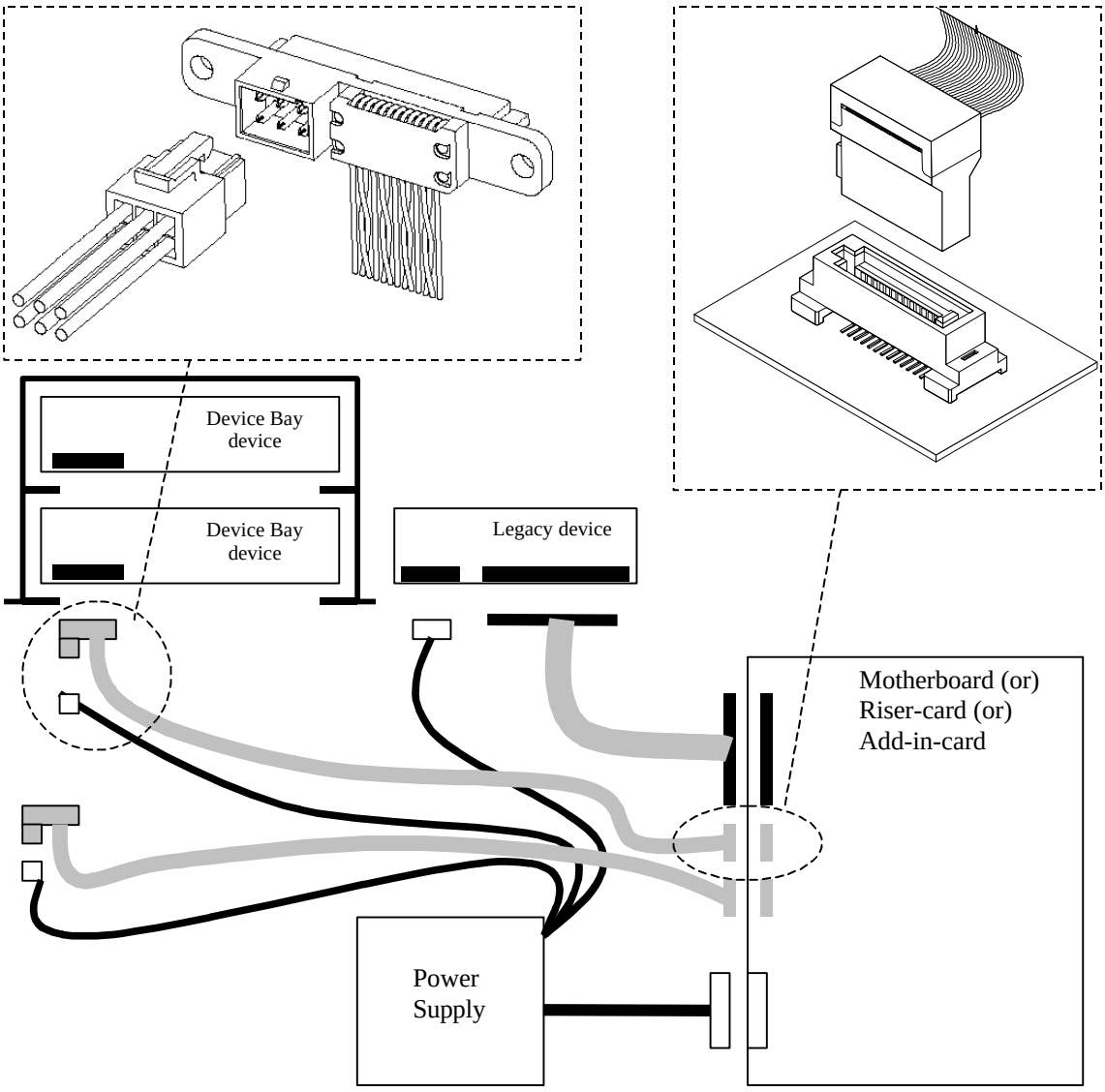


Figure 2. Local Bays implementation example.

2.2. Remote Bays

In a remote bay application, one or more bays can be implemented in a chassis separated from the host system. A remote DB chassis is also known as “remote condo.” One or more remote condos can be connected to a host system. Each remote condo must at least consist of a power supply, a USB-based Device Bay Controller (DBC), power control electronics, a set of user-interface and receptacles for all the bays. The receptacles can be implemented on a DB back panel (Figure 3) or on cables (Figure 4). There will be a pair of self-powered 1394/USB upstream ports on the remote condo interfacing to a pair of 1394/USB downstream ports on a host system. Standard walkup cable assemblies can be used to interface between a remote condo and a host.

2.2.1. PCB Bay Implementation Example

The DBC, power controls, 1394 link/PHY, and USB hubs may be located on the back panel PCB. Figure 3 shows the rear view of the bay and the back panel. The primary advantage for using a back panel for all the bays is no or minimum internal cabling. Consequently, it is easier to achieve good signal integrity for high-speed 1394b differential signals and power distribution. The main challenge is to keep the blind-mate tolerance for all the bays according to the DB spec., especially to support several number of bays.

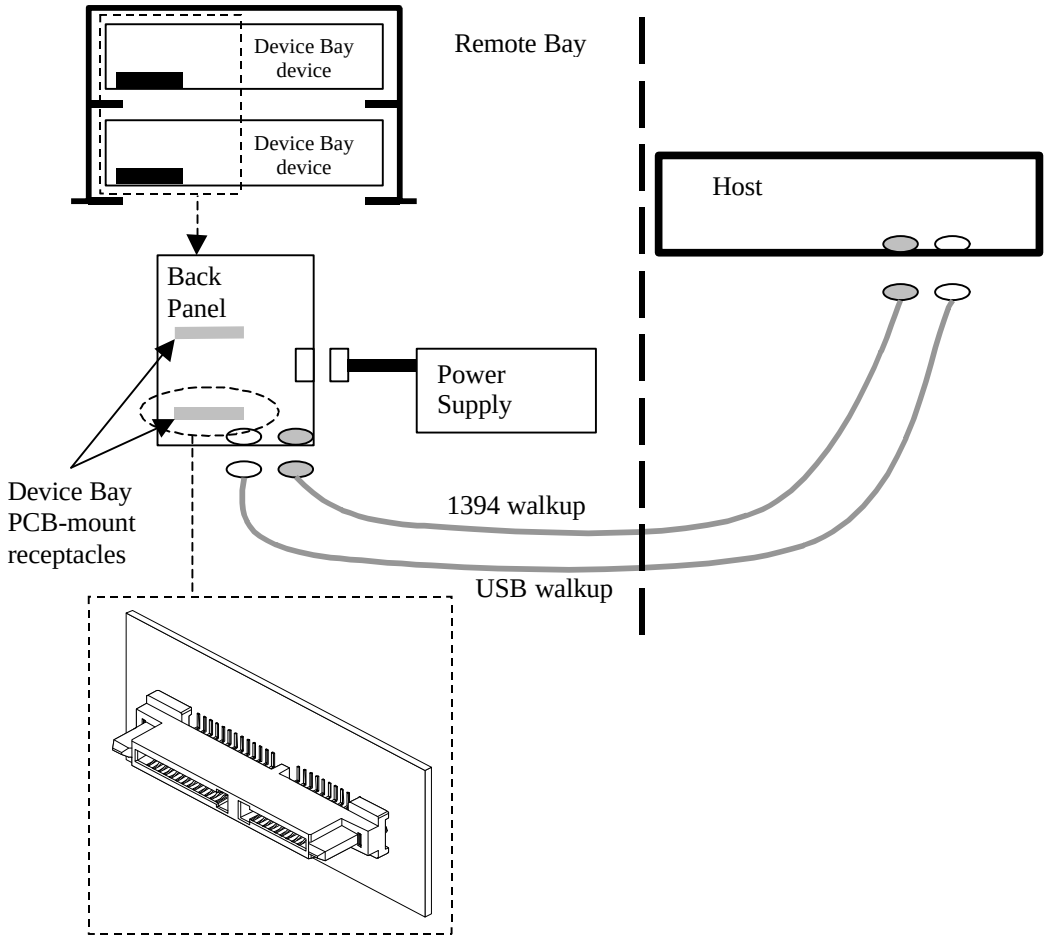


Figure 3. Remote bay implementation example (PCB bay receptacles).

2.2.2. Cable Bay Implementation Example

A USB-based DBC is located on the controller PCB as shown in Figure 4, which also shows the rear view of the bays. One main advantage for using a cable-mounted receptacle for each bay is that there are many ways to float the receptacle to achieve tight blind-mate tolerance for all the bays. One main disadvantage is to manage the cable assemblies to achieve good signal integrity and power distribution.

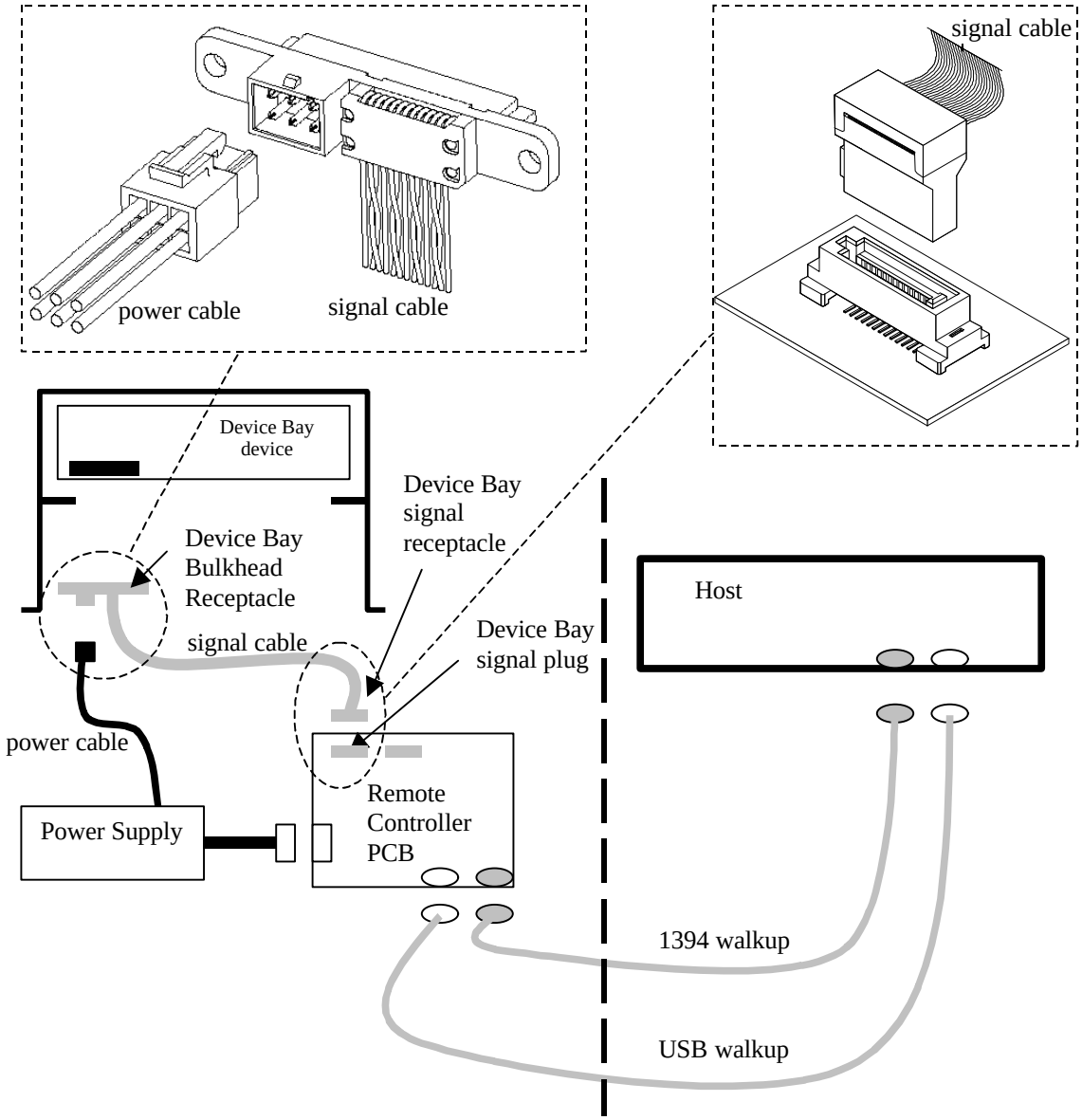


Figure 4. Remote bay implementation example (cable-terminated bay receptacles).

2.3. Internal Device Implementation

A DB device can be semi-permanently mounted inside a host (similar to IDE and SCSI devices). The signal connectivity can be via a cable assembly that runs between a DB device and a PCB, such as the motherboard. The power connector can directly come from the host power supply and directly mated to the receptacle already mated to the device plug as shown in Figure 5.

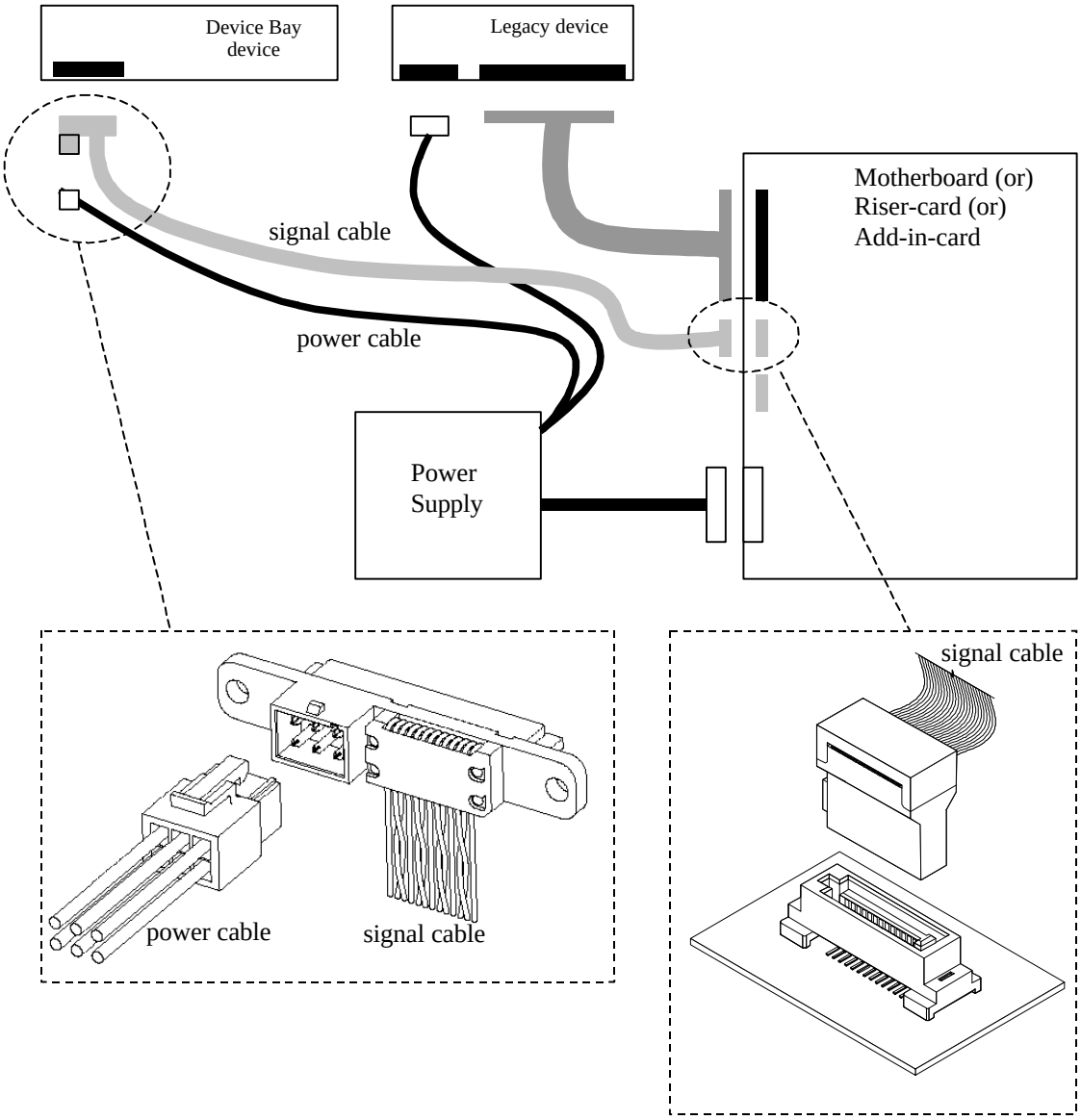


Figure 5. Internal Device implementation example.

3. Connectors and Cables

3.1. Host-Side Device Bay Connectivity

A DB receptacle in a host bay must be positioned in a way that it will enable blind-mating of a DB device when it is inserted in the bay. The DB spec. clearly defines the DB device form factors and corresponding plug locations. There is no explicit description on bay dimensions and how a bay receptacle should be positioned in a bay, since this is implementation dependent. Factors involved in a bay design are airflow, bay guide rails, device insertion mechanism, device ejection/locking mechanism, receptacle type and how it is mounted/terminated, etc. Receptacle mounting might also involve floating in multiple directions depending on mechanical support features for a device in a bay. This section illustrates part drawings and related details whenever appropriate.

3.1.1. Device Bay PCB Receptacle

This section provides details about the mounting feature, termination feature and the dimensions for a PCB mount receptacle, which is also known as the reference design DB receptacle. For details about the receptacle mating features and dimensions, see Section 4 of the DB spec. This receptacle is only an example implementation for PCB mount type primarily for “desktop” applications. A receptacle for portable applications might require right-angle termination pins.

The receptacle reference design is a vertical-mount SMT connector with retaining hardware on the sides to be mounted on a back panel PCB.

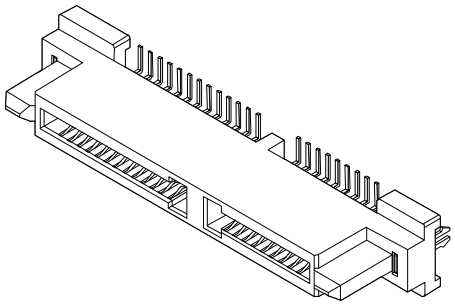


Figure 6. Desktop Bay PCB Mount Receptacle Reference Design

Figure 7 shows the pin assignment where special attention is required to make sure that the 1394 differential signals are correctly routed for a particular implementation. Figure 8 shows the part drawing. Figure 9 shows the PCB footprint.

"Crossing[2]" of the 1394 TPA and TPB signals is accomplished at the connector pair by assigning different pin names on the device plug and the bay receptacle. Therefore, the 1394 differential signal pins A2, A3, A5 and A6 are defined differently between the plug and the receptacle.

For some implementations the 1394 signals may be routed to the bay receptacle directly from the PHY on a PCB. For some other implementations, the 1394 signals may be routed to the bay receptacle after going through a few stages of connector pairs and cable assemblies. In this case, it is important to note that all the connectors within a system enclosure that use the Device Bay connector pin configuration will follow the "Device Bay Receptacle Pin Configuration" (Figure 4-5), regardless of the connector type being a plug or a receptacle. Similarly, there may be cable assemblies within a device, in which case all the connectors within a device that use the Device Bay connector pin configuration will follow the "Device Bay Plug Pin Configuration" (Figure 17), regardless of the connector type being a plug or a receptacle. This is to ensure the proper crossing of the 1394 TPA and TPB signals.

A1	Gnd	Gnd	A14
A2	TPB	Gnd	A15
A3	TPB#	Gnd	A16
A4	Gnd	Gnd	A17
A5	TPA	Gnd	A18
A6	TPA#	Gnd	A19
A7	Gnd	Gnd	A20
A8	1394PRSN#	Gnd	A21
A9	DEV_ACT#	Gnd	A22
A10	USBPRSN#	Gnd	A23
A11	D+	Gnd	A24
A12	D-	Gnd	A25
A13	V_{id}	Reserved	A26
Individual key for the Signal Segment Gap Individual key for the Power Segment			
B1	V_{33}	Gnd	B10
B2	V_{33}	Gnd	B11
B3	V_{33}	Gnd	B12
B4	V_{33}	Gnd	B13
B5	V_{33}	Gnd	B14
B6	V_{33}	Gnd	B15
B7	V_{12}	V_5	B16
B8	V_{12}	V_5	B17
B9	V_{12}	V_5	B18

Figure 7. Device Bay Connector Receptacle Pin-out (Note: All contacts have the same length.)

[2] For the 1394 differential signals, the TPA/TPA# of the device's PHY should be interfaced to the TPB/TPB# of the bay's PHY, respectively. Similarly, the TPB/TPB# of the device's PHY should be interfaced to the TPA/TPA# of *1394-1995 IEEE Standard for a High Performance Serial Bus* specification for details. For the 1394 external (also known as "walkup") connectors/cable, TPA/TPA# of one end goes to TPB/TPB# of the other end, respectively, of the cable.

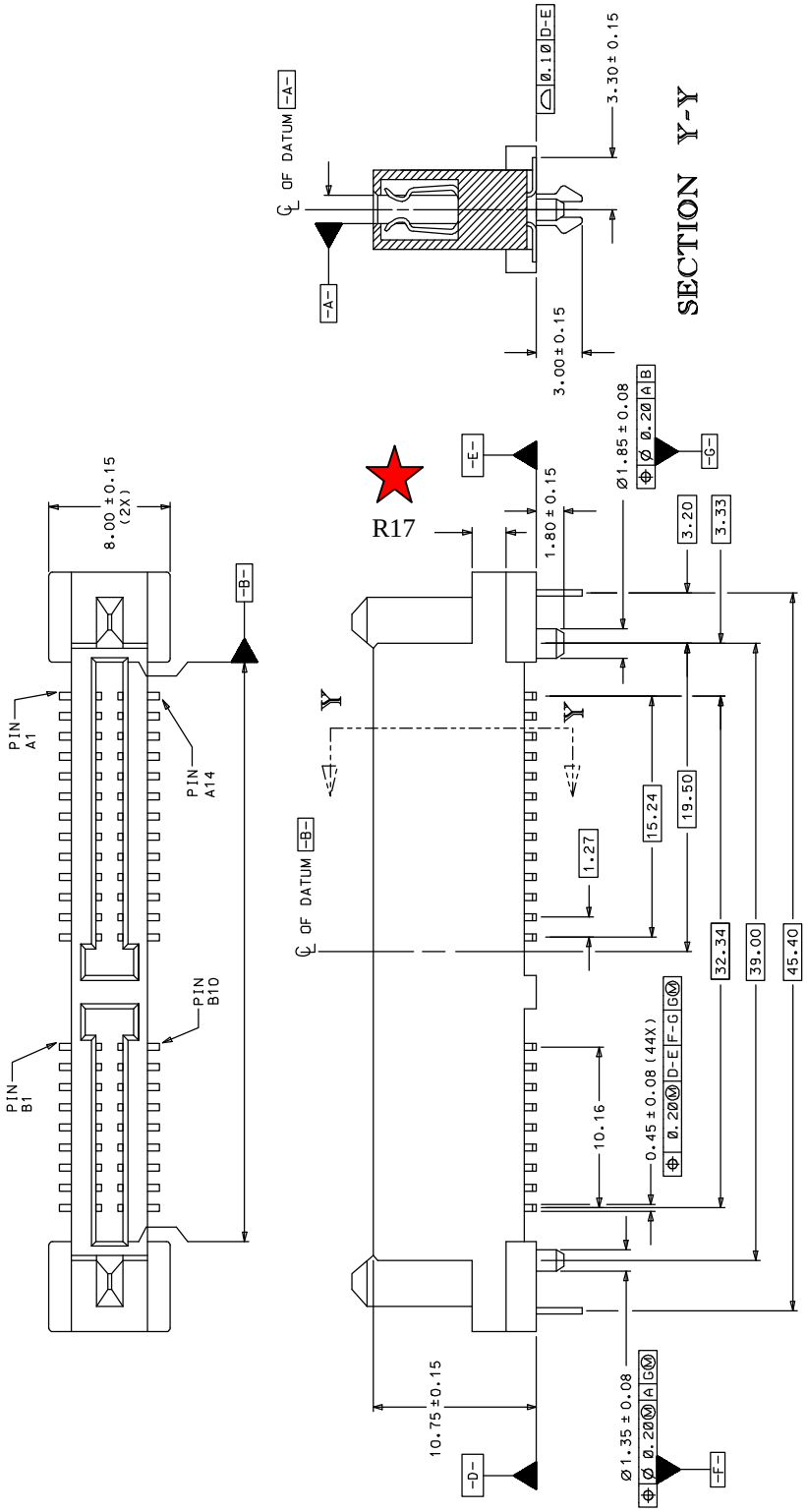


Figure 8. Reference Design Receptacle [see Section 3.1.1.3 for R17].

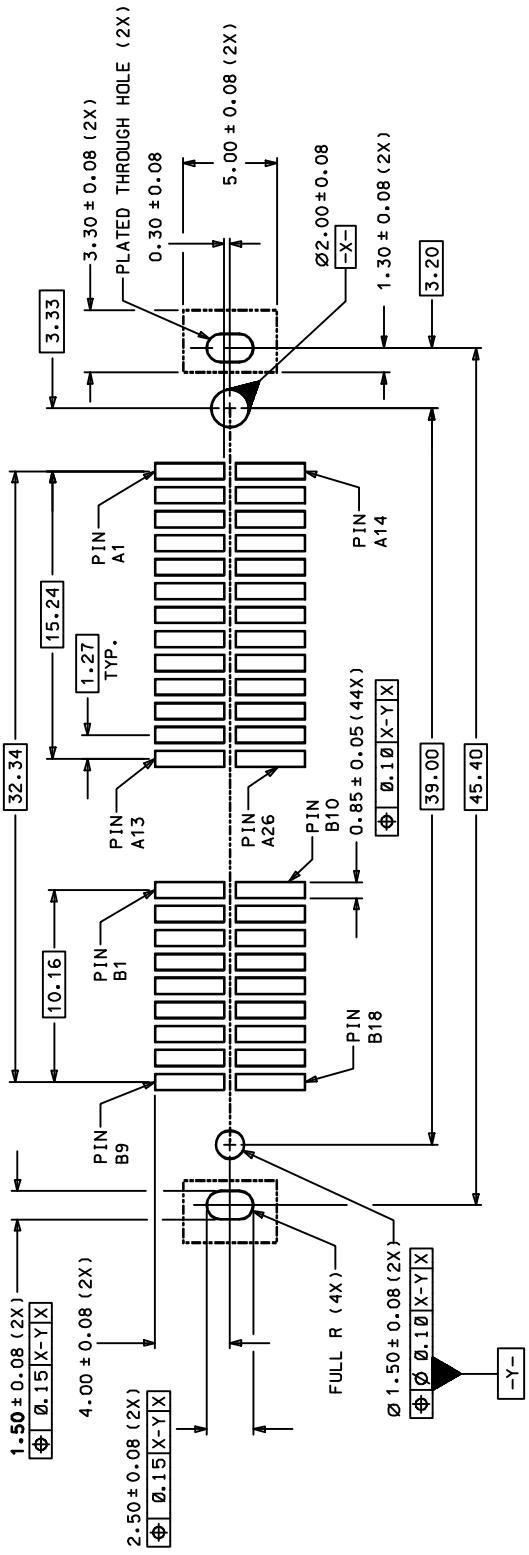


Figure 9. Desktop Bay Receptacle Reference Design Footprint

3.1.1.1 1394 Differential Signal Routing

3.1.1.2 PCB Design

It should be noted that the back surface material of a device might be of metal. Appropriate precautions need to be taken in designing the bay and/or the PCB to prevent shorting of the device back surface with any electrical contacts on the back panel PCB, e.g., through-hole pins of components mounted on the other side of the PCB.

Depending on the bay design a PCB mounted receptacle might need to be mechanically floated for proper blind-mating during a device insertion. In this case, the back panel PCB needs to be floated somehow. Mounting the PCB in the bay from the front (i.e., from the inside) of the bay can be more difficult than mounting the PCB from the back side of the bay. However, mounting from the backside of the bay will require a taller receptacle to accommodate the bay between the receptacle and the device.

Mounting more than one receptacles on a back panel PCB will require close attention in controlling the receptacle mounting tolerances so that all bays will have acceptable blind-mate tolerances for a worst-case condition, where all the bays are populated with devices.

3.1.1.3 Receptacle Shoulder Height

R17 dimension is vendor-dependent. It is important to note that the shoulder height (labeled as R17 in Figure 8) needs to be high enough to accommodate a recessed plug inside a DB32 device. [In the earlier versions (V0.85 and before) of the Device Bay Interface Specification, R17 was defined to be 2.25mm, which we found out to be inadequate for some devices that has worst-case skew for the plug mounting.]

After adding the 2.00mm recess, the 0.5mm recess tolerance and the 0.08mm plastic tolerances for each connector, R17 should be at least 2.68mm. We recommend R17 to be 2.75mm for the PCB mount reference design receptacle.

If a receptacle is to be mounted from the backside of the bay wall, as explained in Section 3.1.1.2, then R17 needs to be much greater than 2.68mm. Some vendors made R17 to be as high as 6.00mm.

3.1.1.4 Other Tips

We have seen samples made by several connector manufacturers and would like to point out things in implementing DB receptacles as follow:

- Fully implement all the features defined in Section 4 of the DB spec.
    - For example, one prototype receptacle did not implement the full “platform” area immediately above the R17 dimension to insert the fork lock metals from the top. This resulted in reduced contact area between the plug’s and the receptacle’s plastic when the connector pair is bottom out at fully-mated condition. This can lead to plastic housing failure at high impact insertion of a device.

It is possible that a system OEM will implement a back panel PCB with a PCB-mount DB receptacle for the bay and a 1394 walkup connector to interface with an internal 1394 port via a short walkup cable. For this case, the system designer must note that the TPA and TPB pairs are crossed within the walkup cable. Therefore, the pair crossing is no longer necessary between the DB receptacle and plug, and the DB receptacle on the back panel PCB will have the same pin configuration as that of the DB plug.

3.1.2. Device Bay "Direct Attach" Bulkhead Receptacle

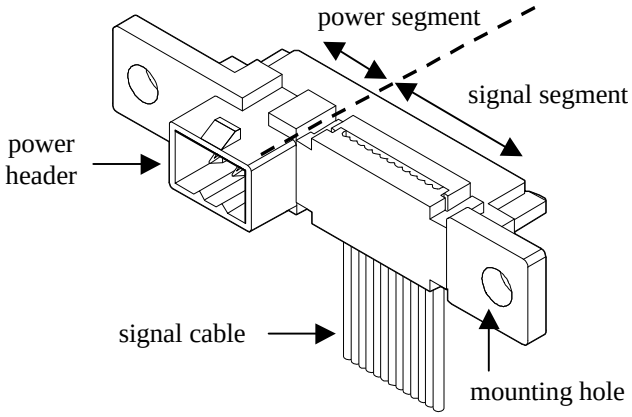


Figure 10. "Direct Attach" Bulkhead Receptacle and Host Power Connector examples.

PCB-mount receptacles are suitable for applications where a system designer wants to locate electronics close to the receptacles and for several bays stacked vertically in a chassis. For some systems, there may be only a few bays where the bays' openings are facing towards different directions of the system. For such a system and for systems with one or two bays, a cable-terminated receptacle is a good alternative. Even implementing several bays in a chassis, cable-terminated receptacles allow bay-independent receptacle floating.

In DB Direct Attach implementation, the signal and the power segments are clearly divided for efficient power and high-speed data cabling. A DB receptacle power segment has 18 contacts where 3 laterally adjacent contacts can be connected together on the rear side to enable large gauge wire/contact termination. One choice is to terminate six 18AWG wires on the rear side of the DB receptacle's power segment and terminate these six wires on any 6-pin power connector. We call that a bulkhead "pig tail" receptacle. Another choice is to terminate six header contacts on the rear side of the DB receptacle's power segment, as shown in Figure 10, so that a 2x3 power receptacle can be directly mated or attached. We call that a bulkhead "Direct Attach" (DA) receptacle. Several off-the-shelf power connectors such as the standard 0.062" and MiniFit Jr. form factors were considered for the DA version. Due to the contact pitch and the limited space behind a DB receptacle, a new form factor was designed within the DB Connector Workgroup. This power connector is called the "6-pin DB Host Power Connector" (see Section 3.1.6.1 for more details).

Though the connector on the other end of the signal cable can be of any gender and type, it is highly recommended to terminate a 26-pin DB signal receptacle, for performance and future interoperability reasons. The cable must support necessary high-speed and current requirements of the signal segment.

The mating portion of a bulkhead DA receptacle must comply with the DB spec. to mate with a DB compliant device. There should be enough clearance all around a bulkhead receptacle to mate with a recessed connector plug in a device (See R17 description in section 4.5.1.3. of the DB spec). The power header portion must comply with the "Device Bay Host Power Connector" specification defined in section 3.1.6.1. of this document, if it is to be mated with a compliant power connector.

It is up to the system designers on how to implement the floating mechanism for the bulkhead DA so that

- it will be presented to the mating device plug with adequate blind-mate tolerances,
- it will ensure a fully-mated condition when an inserted device is in its rest position, and
- it will withstand shocks and vibrations with an inserted device during shipment or operation of the system.

Blind-mate tolerances and fully-mated conditions are defined in the DB spec.

It is up to the system designers and connector manufacturers to implement the mounting features of the bulkhead DA, such as the number, size, shape and positions of the mounting holes, and related mounting hardware. The designers, involved in making the decision on the mounting features, should refer to the DB spec. Chapter 5 to ensure that the

mounting features will not interfere with other bay features, such as the locking and ejecting mechanisms. Figure 11 and Figure 12 (extracted from the DB spec. Chapter 5) show DB32 and its detail rear view, respectively, where the ejector landing and the retention notches areas need to be considered when designing the mounting features for a bulkhead DA receptacle. [The ejector landing area shown in these drawings are incorrectly shown here and in the DB spec. They will be corrected in the next release of the DB spec. and this document.] Additional criteria such as airflow between two vertically adjacent bays and the depth behind the bays may further constrain the mounting feature design.

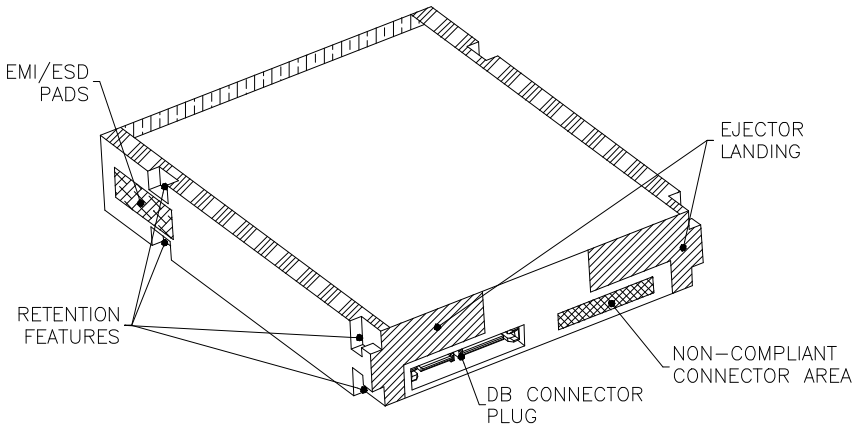


Figure 11. DB32 device.

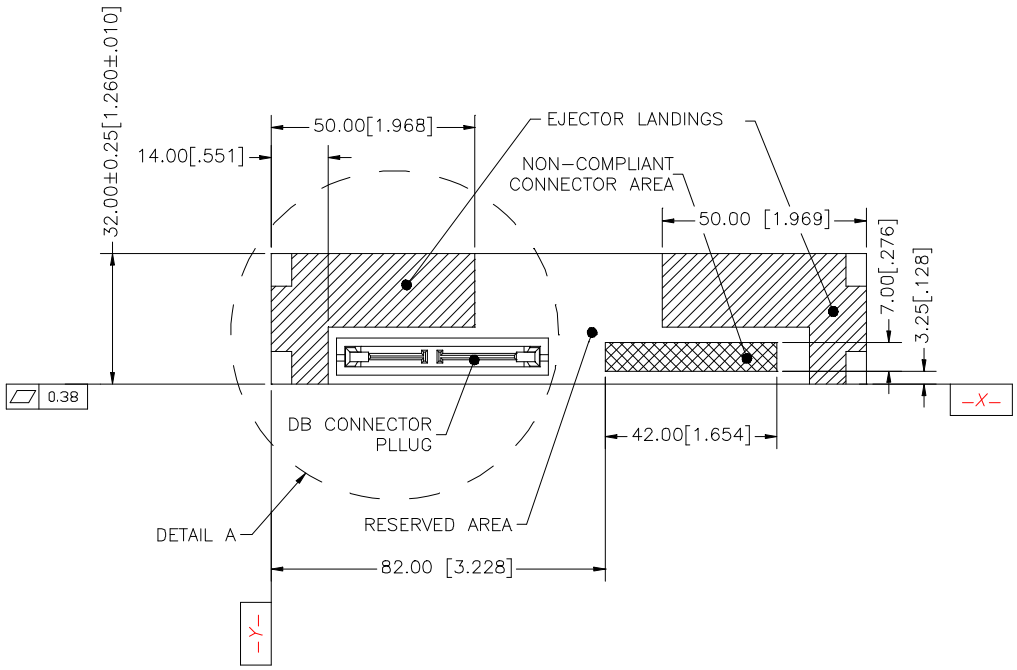


Figure 12. DB32 device rear view details.

A bulkhead DA can also be used for “internal” devices where a device is semi-permanently mounted inside a host chassis, similar to how today’s IDE drives are mounted. In many systems a power supply is located closely behind the internally mounted devices, and the space behind the devices is tight! The fewer the number of cables the better it is in tight spaces, and a bulkhead DA enables easier access for the user to mate the power connectors. It is possible to fix-mount a bulkhead DA on an internal bracket so that a device with DB plug can be plugged in and be secured with mounting screws. If a device is fix-mounted with screws and a bulkhead DA is to be mated (similar to how an IDE cable assembly is mated to a device) then a retaining mechanism for the bulkhead DA can be implemented within the system chassis. For a low-profile power connector for internal devices see Section 3.2.2.

3.1.3. Device Bay 26-Pin Signal Receptacle and Cable

A Device Bay 26-pin signal receptacle is to mate with either a 26-pin signal plug or a 44-pin DB plug in a device. This connector is proposed to be a standard cable-mount connector to interface the "signal segment" of the DB connector.

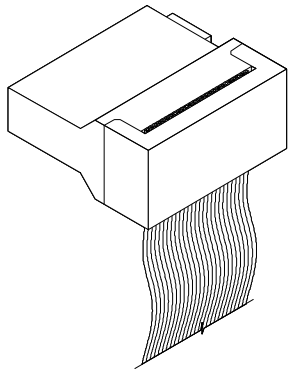


Figure 13. DB 26-pin receptacle example.

Figure 14 shows the pin configuration. It is important to note that this pin configuration is very similar to a microstrip structure[3]. This arrangement gives the connector's 100Ω differential impedance to be very close to a typical PCB's 100Ω differential impedance. Maintaining the A1 through A12 configuration on the cable is preferred to achieve a similar differential impedance value between the connector and the terminating cable.

All the contacts have the same length in the mating area as defined in the DB spec. Connector Chapter. The termination mechanism and the cable types used are implementation dependent, as long as they meet the Device Bay signal performance requirements. For example, only the signal row can be terminated with a 13-wire 0.050" spacing cable. Since the all the pins in the ground row are soldered to the ground plane on the PCB where the plug is mounted, the ground row pins may be bussed together inside the host cable receptacle, and also internally connected to the ground pins in the signal row.

Ground Row		**Signal Row**	
A14	Gnd	Gnd	A1
A15	Gnd	TPB+	A2
A16	Gnd	TPB-	A3
A17	Gnd	Gnd	A4
A18	Gnd	TPA+	A5
A19	Gnd	TPA-	A6
A20	Gnd	Gnd	A7
A21	Gnd	1394PRSN#	A8
A22	Gnd	DEV_ACT#	A9
A23	Gnd	USBPRSN#	A10
A24	Gnd	D+	A11
A25	Gnd	D-	A12
A26	Reserved	V_{id}	A13

Figure 14. DB 26-pin receptacle pin-out.

The signal row (A1 through A13) must always be terminated on the cable. A26 is a reserved pin and it is optional to terminate A26 on the cable[4]. Note that the "ground row" (A14-A25) defined within the signal segment is primarily to control the differential impedance of the 1394 signals, and they are not used for return current per se. As defined

[3] Imagine A14 through A25 to be the "ground plane" and A1 through A12 to be on the "top surface" of a PCB.

[4] A26 on the mating plug located on a PCB is also defined to be a reserved, and it must be a no-connect. Terminating A26 on a cabled receptacle is provided as an option for connector and cable assembly manufacturers' convenience.

in the DB spec., A14 through A25 are required to be grounded inside a device. Since the receptacle's contacts A14 through A25 will be mated to corresponding plug's contacts, connecting A14 through A25 to a ground on the host side via a cable-mount receptacle is optional.

Consequently, a cable might have either 13 or 26 wires depending on the ground terminations within the 26-pin receptacles. However, the contacts in the receptacle mating area must be present to avoid contaminating the plug contacts, regardless of its ground row (A14 through A25) being cable-terminated or not.

Figure 15 illustrates a receptacle and a plug before and after mating for the signal pin A2 and its opposite-positioned ground pin A15 (refer to Figure 14 for the pin out description). In this example, the receptacle's A14 through A25 are not terminated on the cable though there are contacts in the mating area for these positions. When the two connectors are not mated, the receptacle's ground pin A15 is "floating" and plug's ground pin A15 is grounded, Figure 15(a). When the two connectors are mated together as shown in Figure 15(b), the receptacle's A15 becomes grounded via the plug's A15.

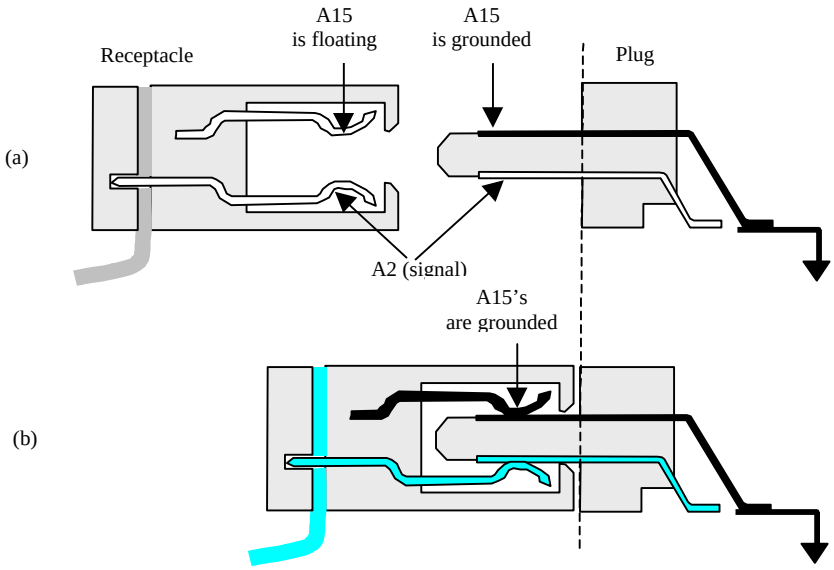


Figure 15. Signal/ground relationship for (a) unmated, and (b) mated contact pairs.

Another important note in designing a DB Signal Receptacle is on how to terminate A13 – the V_{id} pin. The V_{id} termination design will have direct impact on the cable design. The cable terminating to a 26-pin receptacle must accommodate the necessary worst-case current on the A13 pin, since it is part of the entire V_{id} path. For example, for a 36" 28AWG[5] cable carrying 450mA current on the V_{id} wire, the IR loss on the entire cable assembly will be 0.0889V plus the loss through the terminations and the contacts, which will be approximately 0.1V. The V_{id} on the source-end of the cable must be large enough that after factoring all the power supply tolerances and the path losses, the IC(s) on the device will have V_{id} to be 3.0 V minimum. Refer to Section 5 for more details on DB power requirement design tips.

In summary, the signal cable is recommended to be a 13-contact 13-wire termination for pins A1 through A13. The wire gauge is recommended to be 26AWG at least[6] for A13. The cable termination can be accomplished by IDC, solder, or weld techniques, though IDC might be the most cost effective method. The cable may be flat-ribbon, single-and-twist, shielded or unshielded, as long as the electrical requirements[7] defined in the DB spec. and the 1394 signal requirements defined in the 1394 spec. are met.

[5] A 28AWG wire has 0.0653Ω loss per linear feet.

[6] A 13-conductor cable assembly can be implemented with 28AWG for A1 through A12, and 26AWG for A13.

[7] The IR loss for the V_{id} and the electrical parameters for the differential signals especially for 1394b.

3.1.4. Device Bay Signal Plug

The DB signal plug is primarily meant for interfacing the DB signal via a cable-terminated DB signal receptacle. The DB signal plug is a 26-pin vertical PCB mount connector. This connector is proposed to be a standard PCB-mount connector to interface the "signal segment" of the DB connector.

The polarization features are identical to the signal segment half of the DB plug, except the 26-pin plug has a shroud because of a possible life V_{id} pin. The 44-pin DB plug has staggered contact pin lengths in the mating area for hot plug purposes. Since the 26-pin signal plug will not need to be hot plugged, the contact lengths of the signal plug do not have to be staggered. The signal plug should accommodate the raised blind-mate ears implemented on some of the 26-pin signal receptacles.

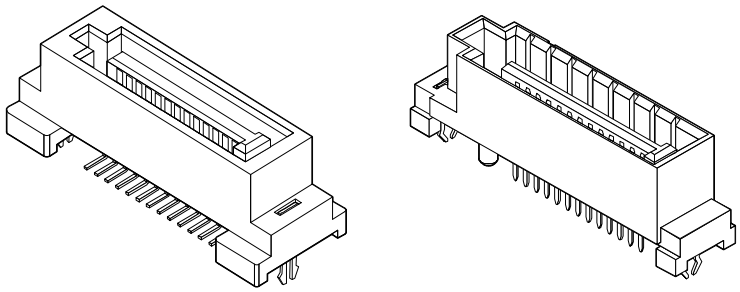


Figure 16. 26-pin DB signal plug (SMT and through-hole vertical-mount versions).

Ground Row		Signal Row	
A14	Gnd	Gnd	A1
A15	Gnd	TPB+	A2
A16	Gnd	TPB-	A3
A17	Gnd	Gnd	A4
A18	Gnd	TPA+	A5
A19	Gnd	TPA-	A6
A20	Gnd	Gnd	A7
A21	Gnd	1394PRSN#	A8
A22	Gnd	DEV_ACT#	A9
A23	Gnd	USBPRSN#	A10
A24	Gnd	D+	A11
A25	Gnd	D-	A12
A26	Reserved (No Connect)	V_{id}	A13

Figure 17. 26-pin DB signal plug pin-out.

It is important to note that the signal plug's pin-out, as shown in Figure 17, is the same as that of the 44-pin DB receptacle's signal segment pin-out defined in the DB spec. Several ground pins are used to achieve the necessary impedance levels, especially for the 1394b differential signals.

Figure 18 shows the mating area specification to implement a 26-pin signal plug. Dimensions for a 26-pin signal receptacle can be derived from this figure. It should be noted the mating dimensions of the 26-pin signal plug is the same as the 44-pin device plug defined in the DB spec. except the followings:

- overall length dimension, and
- uniform contact lengths.

Similarly, it should be noted the mating dimensions of a 26-pin signal receptacle is the same as the 44-pin bay receptacle defined in the DB spec. except the followings:

- overall length dimension, and
- the plastic "bumps" for cable retention.

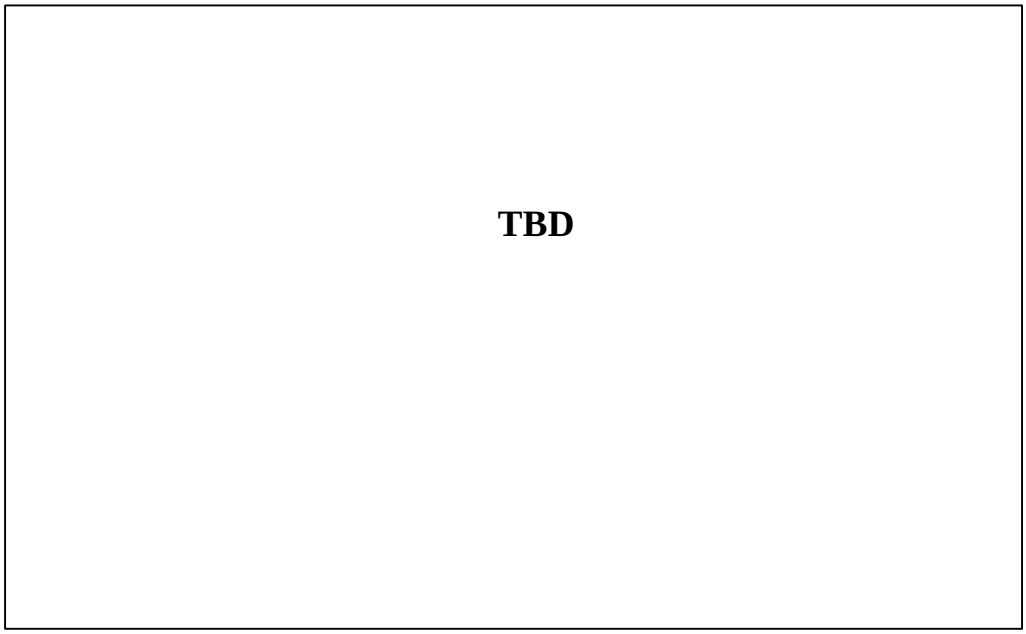


Figure 18. 26-pin signal plug mating area specification.

3.1.5. Notes for the 26-Pin Signal Plug and Receptacle

3.1.5.1 26-Pin Signal Receptacle's Multiple Applications

The 26-pin signal receptacle is intended to be used either with a 26-pin signal plug (for host PCB interface) or a 44-pin device plug (for internal device interface). When a 26-pin signal receptacle is used for internal device interface, it will have to be coexist with a 18/6 power receptacle on a 44-pin device plug.

3.1.5.2 Using Device Bay Signal Connectors for Non-Device Bay Applications

It is possible that some system designers will use DB 26-pin connectors and cable assemblies for non-DB applications where the pin assignment may be different. One application that we have seen is to route one set of 1394 signals and two sets of USB signals from one PCB to another PCB within a chassis. The following are the two main concerns for this application:

1. Mistakenly mating the non-DB cable assembly on a DB connector, or vice versa –
   It is important to note that this 26-pin signal plug has polarization but does not have "keying"[8]. If one or more 26-pin plugs are used to interface with DB devices and a 26-pin plug is also used for other applications[9] with a different pin-out, appropriate measures must be taken so that the V_{id} on the 26-pin plugs for DB application will not be shorted.

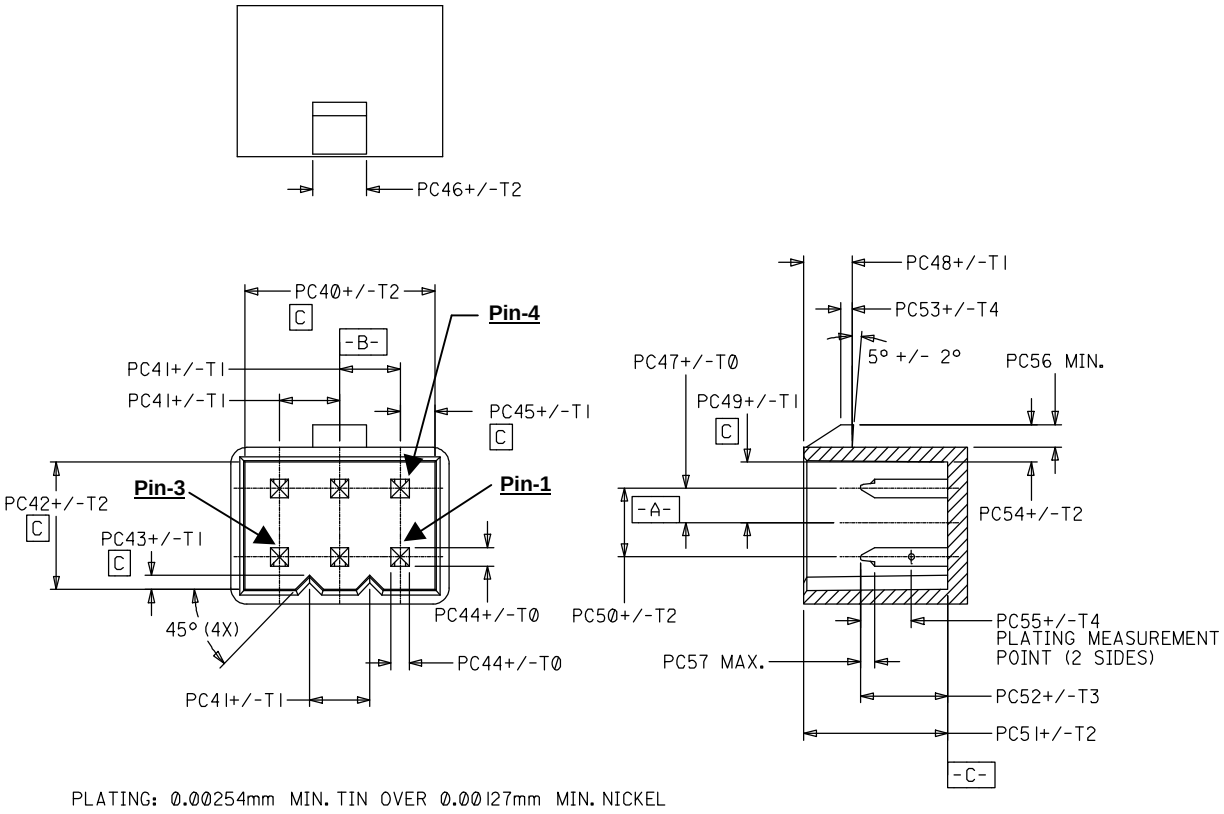
2. Incompatible DB signal cable assembly wire termination –
   Some cable assemblies initially meant for DB applications might not have pin A14-A26 terminated on the cable.

[8] For example, when there are same size connectors with different pin-outs within a system using 0.1" centered pin headers, a header pin could be cut to key with a corresponding blocked pin on a receptacle.

[9] Some users have shown interests in using this 26-pin connector in non-Device Bay applications with pin configurations different from Figure 17. For example, interfacing 1394 and USB signals (and power) from the motherboard to a system front-panel.

3.1.6. Device Bay Host Power Header Specification

This connector is proposed to be a standard 6-pin DB host power header connector.



	mm		mm		mm
PC40	12.00	**PC49**	3.70	**T0**	0.05
PC41	3.81	**PC50**	4.20	**T1**	0.08
PC42	7.80	**PC51**	9.10	**T2**	0.10
PC43	0.89	**PC52**	5.50	**T3**	0.15
PC44	1.14	**PC53**	0.70	**T4**	0.20
PC45	2.19	**PC54**	2.30		
PC46	3.40	**PC55**	3.20		
PC47	2.10	**PC56**	1.40		
PC48	3.06	**PC57**	1.02		

Figure 19. DB Host Power header mating area.

The DB 6-pin Host Power header can be implemented in several forms. For example,

- Integrated directly on the backside of a receptacle as shown in Section 3.1.6.1.,
- A cable-mount version as shown in Section 3.1.6.2,
- A PCB-mount version (not shown).

3.1.6.1 Device Bay 6-Pin Host Power Header (Bulkhead Direct Attach)

DB Host Power connector header mating area detail information is shown in Figure 19. The power receptacle (with female or socket contacts), described in 3.1.7, can be extrapolated from Figure 19. Existing off-the-shelf female contacts[10] may be used in a plastic housing complying to Figure 19. Square contacts were chosen for best interoperability. The horizontal pin spacing (PC41 in Figure 19) was chosen to be 0.150" (3.81mm), to enable easy implementation of "Direct Attach" Bulkhead connectors[11].

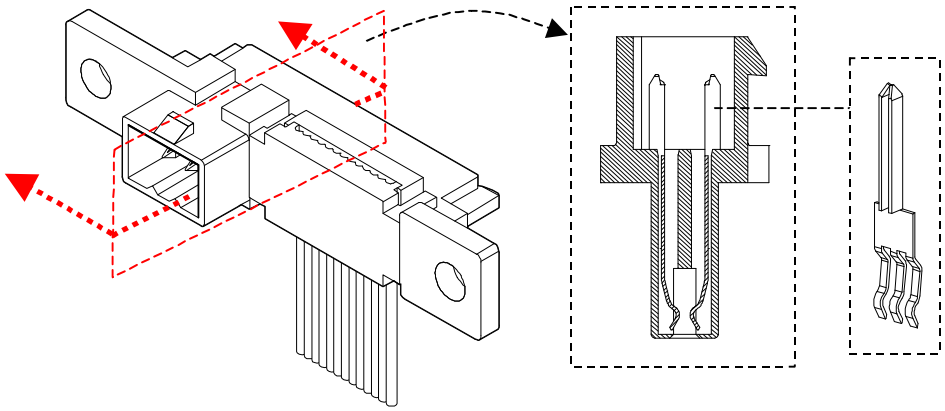


Figure 20. 6-pin DB power receptacle and an integrated header on a bulkhead receptacle example.

Note that the DB 44-pin receptacle has 18 pins for the power segment and the DB Host Power connector has 6 pins. Therefore a bulkhead receptacle with an integrated power header needs a 6-to-18 contact translation, which can be done by a "pitch-fork" design as shown in Figure 20 (cross-section view and extracted pitch-fork contact in dotted-line boxes). Pin configuration in the power segment of DB receptacle was designed to support such an implementation. Three contacts can be grouped or bussed together on the DB bulkhead receptacle bay-mating side as shown in Figure 21. In addition, the 0.150" horizontal contact spacing of the 6-pin DB Host Power connector was designed to enable a single mold design for all the six pitch-fork contacts.

4 5 6

B10	Gnd	V_{33}	**B1**
B11	Gnd	V_{33}	**B2**
B12	Gnd	V_{33}	**B3**
B13	Gnd	V_{33}	**B4**
B14	Gnd	V_{33}	**B5**
B15	Gnd	V_{33}	**B6**
B16	V_5	V_{12}	**B7**
B17	V_5	V_{12}	**B8**
B18	V_5	V_{12}	**B9**

1 2 3

Figure 21. DB Host Power 6-to-18 pin translation for the pitch-fork contacts.

In Figure 21, the 18-pin configuration is shown within the table. The 6-pin configuration is shown in dotted-line boxes on both sides of the table. Each pin of the 6-pin configuration is shown next to the corresponding 3-pin group of the 18-pin configuration.

[10] For example, Molex's MiniFit Jr. compatible contacts.

[11] Because of this 0.150" pitch, off-the-shelf power connectors such as Molex's MiniFit Jr. or 0.062" Power connectors could not be used with requiring multiple designs for the pitch-fork contacts for "direct plug" Bulkhead connectors.

3.1.6.2 Device Bay 6-Pin Host Power Header (Cable-Mount)

DB 6-pin Host Power header can be implemented for a cable-mount version. As an alternate solution to a Direct Attach Bulkhead receptacle, a cable terminated 6-pin Host Power header can be "pig-tailed" behind a bulkhead connector. How the wires are actually terminated on the bulkhead power pins is implementation dependent, e.g., soldering, crimping, etc. Yet another alternative is to use a 6-pin Host Power header wired to an 18/6 Host Power receptacle as shown in Section 3.2.2.

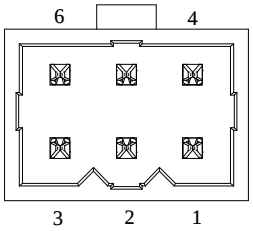


Figure 22. Host Power header pin orientation.

1	3.3V (Brown)	Gnd (Black)	**4**
2	3.3V (Brown)	Gnd (Black)	**5**
3	12V (Orange)	5V (Red)	**6**

Figure 23. Host Power header pin-out (recommended wire colors for wire-to-wire versions).

3.1.7. Device Bay 6-Pin Host Power Receptacle (Cable-Mount)

A DB Host Power receptacle implementation can be derived from this Host Power header specification shown in Section 3.1.6.1. This connector is proposed to be a standard 6-pin DB host power receptacle connector.

Most today's PC power supplies support 3.3V, 5V and 12V for DB power requirements. A system implementation may run a set of six 18AWG wires directly from the host power supply to a wire-to-wire DB 6-pin Host Power receptacle for each bay to be supported.

An alternate implementation may be to run the six power wires from a motherboard to terminate on a dB 6-pin Host Power receptacle. For this implementation, one would need to mount another power connector header on the motherboard which can be of any type, plus possible additional power wires between the host power supply and the motherboard. Note that each stage of connector pair and sets of wires will introduce IR losses on each power supply voltage. It is the system designer's responsibility to ensure that the voltage presented at the bay receptacle is

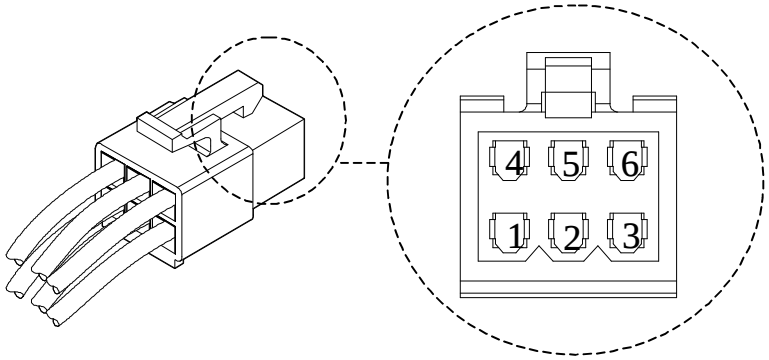


Figure 24. DB 6-Pin Host Power receptacle example and pin orientation.

1	3.3V (Brown)	Gnd (Black)	**4**
2	3.3V (Brown)	Gnd (Black)	**5**
3	12V (Orange)	5V (Red)	**6**

Figure 25. Host Power receptacle pin-out (recommended wire colors for wire-to-wire versions).

3.2. Host-Side “Internal Device” Connectivity

A DB device or a device with a DB plug can also be fixed-mounted inside a system, similar to how today’s IDE/SCSI internal storage device are mounted. This section describes example implementations on how interconnectivity for such a device can be achieved.

3.2.1. Bulkhead and 6-Pin Power Receptacles

The bulkhead receptacle is the same connector described in Section 3.1.2. It is up to the system designers on how to retain the bulkhead receptacle. For example, the bulkhead can be mounted on an internal bracket where a device can be plugged in and then being secured, or a bulkhead can be plugged to a secured device and then some sort of retaining mechanism “holds” the bulkhead in place.

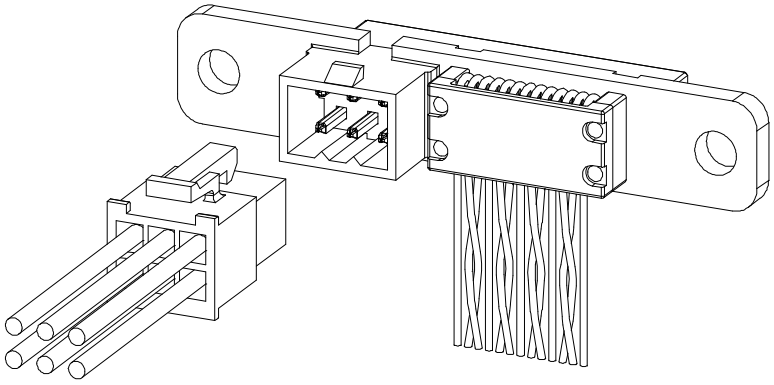


Figure 26. A 6-pin power receptacle mating to a Bulkhead DA power header.

3.2.2. 26-Pin Signal and 18/6 Host Power Receptacles

The 26-pin signal receptacle is shown in Figure 27, and it is the same connector described more detailed in Section 3.1.3.

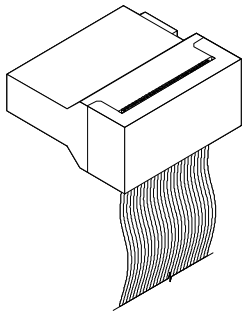


Figure 27. 26-pin signal receptacle.

The 18/6 Host Power receptacle is directly mateable to a 44-pin device plug and has a mean to terminate 6 power wires. The 18-to-6 pin translation is done by bussing 3-pin groups of the 18 pins in the mating area to each power terminal. In Figure 28, a pitch-fork contact is shown inside a dotted-line box (the termination towards the 6-pin side is blocked off to illustrate that it is implementation-dependent, e.g., a solder or a crimp type). Figure 29 shows the 3-pin grouping for each power terminal, in dotted-line boxes on each side of the table. The power terminal pin out is 1-to-1 correspondent to the 6-pin power connectors described in Section 3.1.6 and 3.1.7. The power cable termination may be of IDC, crimp, or solder type. All the mating contacts in the receptacle have the same length in the mating area, as defined in the DB spec.'s Connector Requirements.

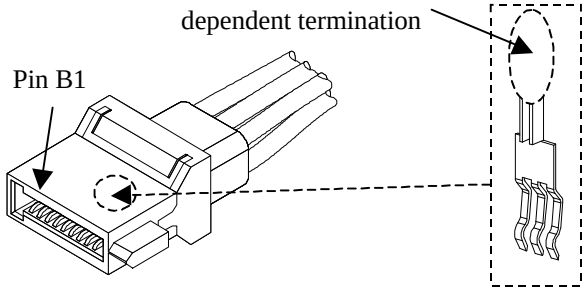


Figure 28. 18/6 Host Power receptacle.

4 5 6

B10	Gnd	V_{33}	**B1**
B11	Gnd	V_{33}	**B2**
B12	Gnd	V_{33}	**B3**
B13	Gnd	V_{33}	**B4**
B14	Gnd	V_{33}	**B5**
B15	Gnd	V_{33}	**B6**
B16	V_5	V_{12}	**B7**
B17	V_5	V_{12}	**B8**
B18	V_5	V_{12}	**B9**

1 2 3

Figure 29. 18/6 Host Power Receptacle pin-out.

The 6-pin Host Power header can be terminated on the other end of the wires of the 18/6 Host Power receptacle (as shown in Figure 30). This method will introduce additional voltage drop but will allow the power supply to have one type of connector – the DB 6-pin Host Power receptacle – for both DB bays and internal devices. There will also be cost adder due to the additional power cable assembly.

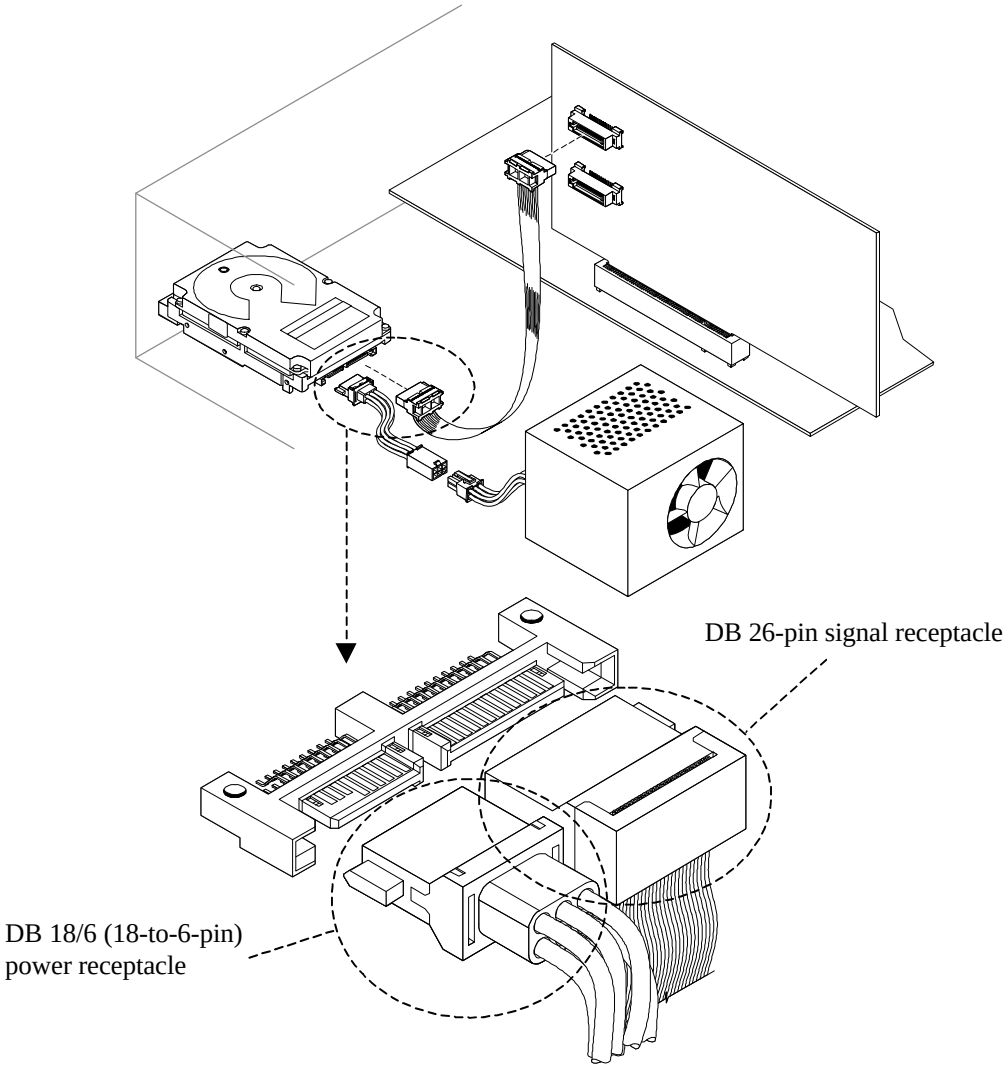


Figure 30. Separate power and signal cable assemblies mating to a device plug.

The power wires from the 18/6 Host Power receptacle can even come directly from the power supply. However, this will require making this 18/6 connector to be a requirement for a "standard" power supply for the PC industry, which might not be a good idea because this 18/6 connector will not be able to used with the bulkhead receptacle for the DB bays.

3.3. Device-Side Connectivity

3.3.1. Device Bay Device Plug

The plug connector for a Device Bay device is a 90-degree mount SMT connector, with mechanical retention holes. The plug can be securely mounted on the device by attaching screws through the plug's mounting holes, the device PCB, and the device chassis.

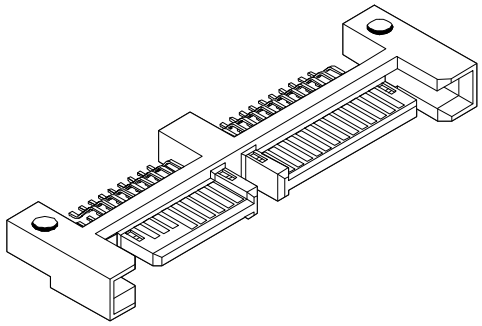


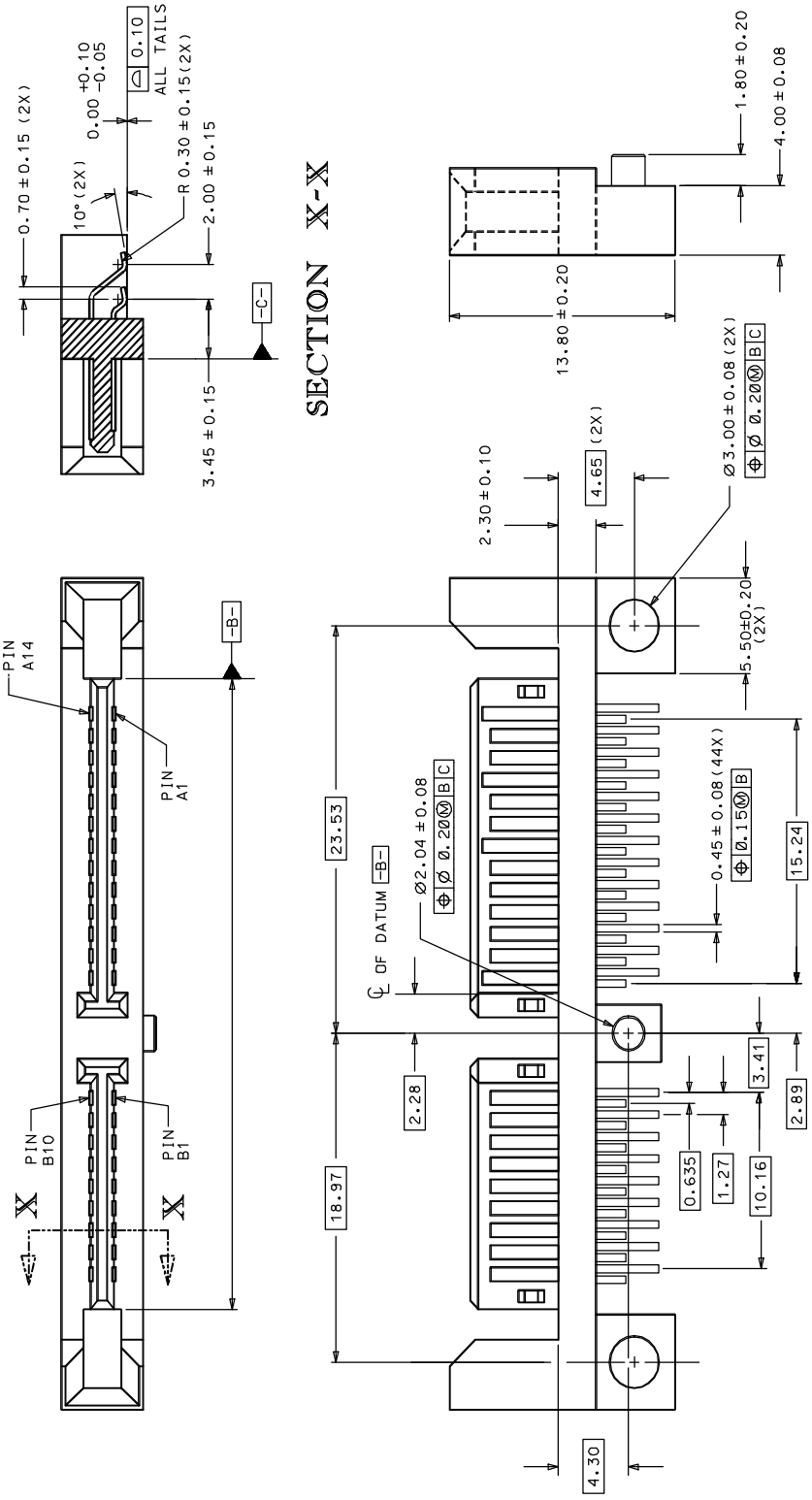
Figure 31. Device plug example.

A14	Gnd (1st mate)	Gnd (1st mate)	A1
A15	Gnd (1st mate)	TPA	A2
A16	Gnd (1st mate)	TPA#	A3
A17	Gnd (1st mate)	Gnd (1st mate)	A4
A18	Gnd (1st mate)	TPB	A5
A19	Gnd (1st mate)	TPB#	A6
A20	Gnd (1st mate)	Gnd (1st mate)	A7
A21	Gnd (1st mate)	1394PRSN#	A8
A22	Gnd (1st mate)	DEV_ACT#	A9
A23	Gnd (1st mate)	USBPRSN#	A10
A24	Gnd (1st mate)	D+	A11
A25	Gnd (1st mate)	D-	A12
A26	Reserved	V_{id} (1st mate)	A13
Individual key for the Signal Segment Gap Individual key for the Power Segment			
B10	Gnd (1st mate)	V_{33}	B1
B11	Gnd (1st mate)	V_{33}	B2
B12	Gnd (1st mate)	V_{33}	B3
B13	Gnd (1st mate)	V_{33}	B4
B14	Gnd (1st mate)	V_{33}	B5
B15	Gnd (1st mate)	V_{33}	B6
B16	V_5	V_{12}	B7
B17	V_5	V_{12}	B8
B18	V_5	V_{12}	B9

Figure 32. DB plug pin-out.

For the high end of the 1394b differential signals (e.g., 3.2Gbps) it is desired to keep the signal sequence in the signal segment is maintained on the solder pads to minimize the impedance discontinuity between the PCB and the connector. The followings are two ways to maintain the signal sequence – not interleaving the solder tail pins in the "ground row" (A14-A25) and the "signal row" (A1-A13) in the signal segment:

- Terminate A1-A26 on the same side of the PCB, but stagger the pads for A1-A13 and the pads for A14-A26 in different rows, as shown in Figure 33.
- Terminate A1-A13 on one side of the PCB and terminate A14-A26 on the other side of the PCB.



IMPORTANT NOTE

The connector mounting feature and the "staggered" or "two-row" PCB termination pins are shown here as an example implementation. This staggered pin version is available from some connector vendors. The "inline" or "one-row" termination version for the reference design plug is also available from some connector manufacturers. The actual part drawing and a corresponding PCB footprint drawing should be acquired directly from the connector manufacturers.

Figure 33. Device plug reference design dimensions

3.3.2. Device Plug Mounting

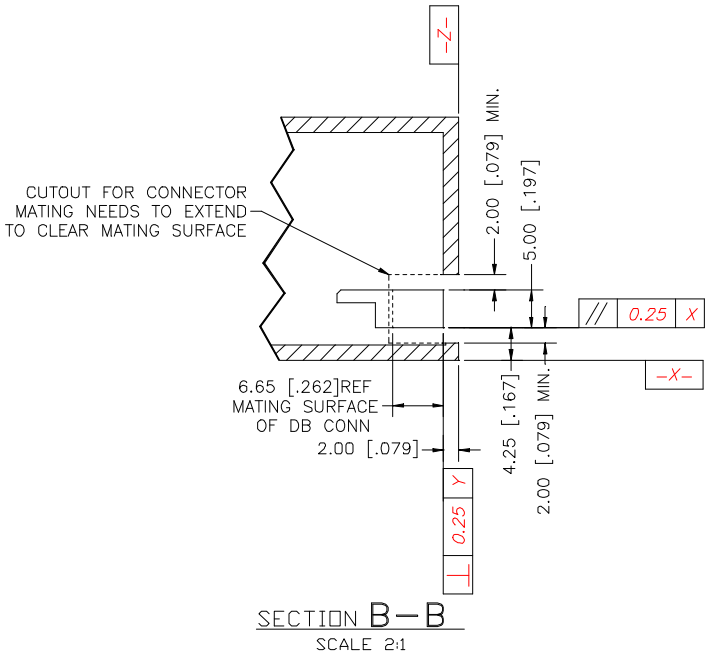


Figure 34. Device plug location.

Perpendicularity controls the plug skew for one axis or with respect to a vertical plane (datum Z in Figure 34). Parallelism controls the plug skew for two axes or with respect to a horizontal plane (datum X in Figure 34). Perpendicularity and Parallelism tolerances are both defined to be 0.25mm each for a device plug's maximum skew tolerances with respect to the side surface and the bottom surface, respectively, of a device enclosure.

In chapter 4 of the DB spec. the followings were defined for a mated connector pair without considering any skews:

- contact wipe: 1.46mm
- horizontal blind-mate tolerance: ±2.00mm
- vertical blind-mate tolerance: ±1.95mm

Assuming the receptacle does not align to the plug's skew, and considering the worst-case skews for a connector plug, the remaining tolerances for a to-be mated pair are as follow [see Figure 36]:

- horizontal blind-mate tolerance: ±1.99mm
- vertical blind-mate tolerance: ±1.85mm

And the remaining tolerance for a mated pair is as follow:

- contact wipe: 1.29mm [shown as W in Figure 35]

Section 3.3.2.1 and 3.3.2.2 explains how the perpendicularity and the parallelism tolerances were derived, and their related trade-off parameters – contact wipe and blind-mate tolerance, respectively. It is up to a system designer to decide how much of the contact wipe and blind-mate tolerances will be left for the application. See Section 5 of the DB spec. for more details on the connector plug mounting location with respect to the device enclosure.

3.3.2.1 Perpendicularity Tolerance Analysis

The perpendicularity tolerance is defined as shown in Figure 35, so that the plug connector skew can be measured physically (before the device is completely assembled). The skew angle is difficult to be measured physically. The DB spec. defines the perpendicularity tolerance to be 0.25mm. The following table shows the trade-off between the perpendicularity tolerance and the contact wipe.

Tolerance Condition	Skew Angle "B" (degrees)	Perpendicularity "A" (mm)	Contact Wipe "W" (mm)
Nominal	0.00	0.00	1.85
Minimum	0.00	0.00	1.50
	0.25	0.21	1.32
	0.30	0.25	1.29
	0.45	0.38	1.18
	0.50	0.42	1.15
	1.00	0.84	0.80

Assumptions:

1) The connectors are mated as fully as possible (they serve as the stop in the system) as described in Section 5.3.2.2 of the Device Bay Interface Specification.
2) Skew / perpendicularity of the device relative to the receptacle "backplane" has not been included.

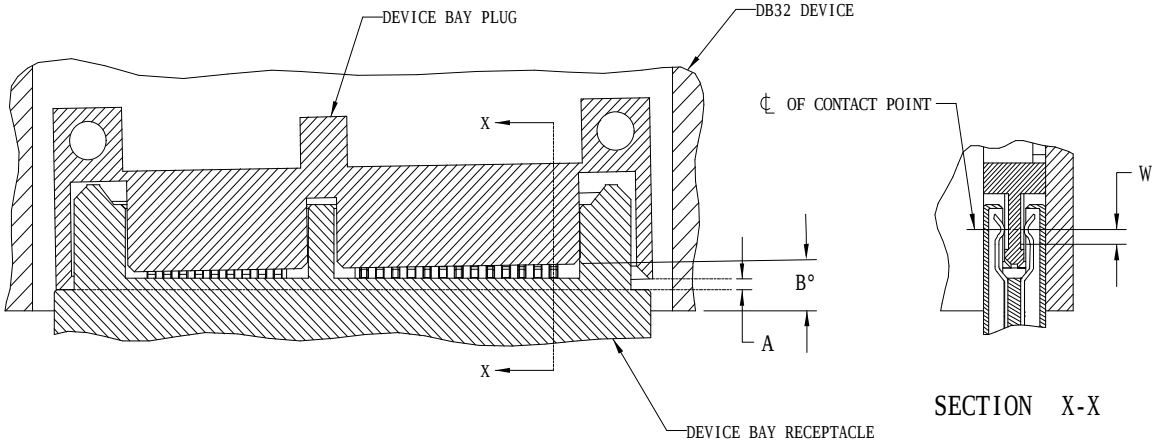


Figure 35. Perpendicularity skew.

3.3.2.2 Parallelism Tolerance Analysis

The parallelism tolerance is defined as shown in Figure 36, so that the plug connector skew can be measured physically. The skew angle is difficult to be measured physically. The receptacle lead-in's shown in Figure 36 represent the positions for the blind-mate ear "tips" of a non-skewed receptacle. Note that the parallelism skew applies to the entire horizontal plane, i.e., both mating and termination ends, of the plug. The DB spec. defines the parallelism tolerance to be 0.25mm. The following table shows the trade-off between the parallelism tolerance and the blind mate tolerance.

Tolerance Condition	Skew Angle "D" (degrees)	Parallelism "C" (mm)	Blind Mate Horizontal Axis "E" (mm)	Blind Mate Vertical Axis "F" (mm)
Nominal	0	0	2.40	2.15
Minimum (without True Position)	0	0	2.20	2.13
Minimum (with True Position)	0	0	2.00	1.98
Minimum (with True Position)	0.25	0.21	1.99	1.87
	0.30	0.25	1.99	1.85
	0.45	0.38	1.98	1.79
	0.50	0.42	1.98	1.77
	1.0	0.84	1.96	1.56

Assumptions:

1) The connectors are mated as fully as possible (they serve as the stop in the system) as described in Section 5.3.2.2 of the Device Bay Interface Specification.
2) Skew / perpendicularity of the device relative to the receptacle "back-plane" has not been included.

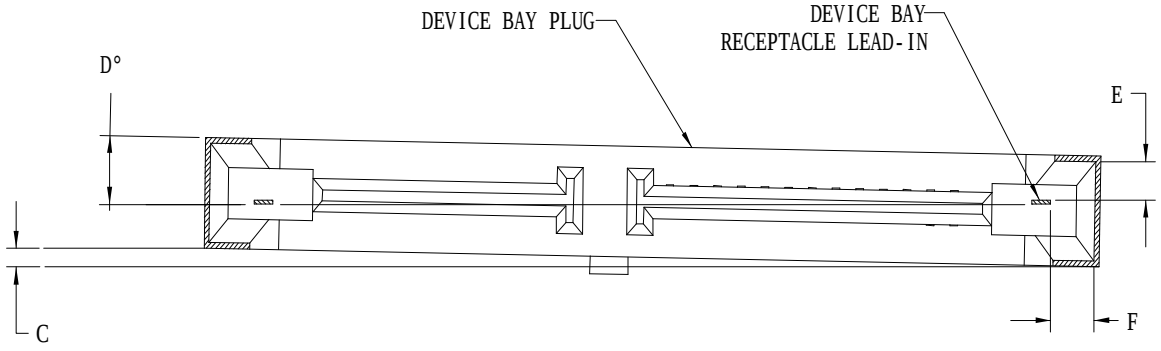


Figure 36. Parallelism skew.

3.4. A Summary of Tips for Cables and Connectors

1. PCB-mount receptacle selection should account for all the clearances (if any) between the PCB and the back surface of a device, plus the worst-case recess of the device plug. [Also see Section 3.1.1.]

2. For PCB-mount receptacles, make sure that there are no electrical contacts protruding towards the inside of the bay on the PCB. Many DB devices have metal surface on the back side. Any protruding contacts with a voltage (e.g., through-hole pins of discrete components or connectors) can be short-circuited when a device is inserted and pushed in to positively latched with the locking mechanism. Use proper insulation if protruded contacts cannot be avoided (Cross check with tip #2).

3. After a device is fully inserted, the ejection springs will be pushing a device out while the locking mechanism will be holding the device back. At this device-equilibrium or -resting state, make sure that the device plug and the receptacle contacts will have enough wipe under a worst-case condition. Independently forcing the receptacle onto the plug can significantly improve the fully mated condition for the Device Bay connector pair, but this can only be effectively done for cable-mount receptacles.

   For an inserted device, the contact wipe will depend on the mechanical stability of the device in a bay and the mating mechanism for the connector pair. If a device is stabilized inside a bay (e.g., by means of locking and ejecting mechanisms) and the bay receptacle is forced onto the mating device plug, then the contact wipe will be virtually constant while the device in the bay. Otherwise, the contact wipe can be varying due to the movement of the device in the bay. Excessive varying of the contact wipe under a mating condition can cause the contact plating to wear out prematurely which can lead to unreliable electrical connection.

4. Mounting of all the bay receptacles must comply to the blind-mate tolerance defined in the DB spec. If a receptacle is floated in a bay it must have some sort of “self-alignment” or “self-centered” after a device is completely demated.

5. If V_{id} is to be supported via the signal cable, the wire guage must be able support V_{id} current adequately for a chosen length. Consequently, the receptacle connectors that will be terminating on the signal cable should have appropriate termination provision to support the necessary wire gauge cable(s).

6. If V_{id} is to be “enabled” on a backplane PCB then the signal cable only needs to support the V_{id}-enable instead of V_{id} itself. In this case the wire guage is not as critical as the previous case (that supports V_{id} directly on the cable). It is the system designer’s responsibility to ensure the V_{id} (voltage and current) enabled on the PCB to comply with the DB spec.

3.5. Device Bay Interconnectivity Reference Designs

The following connectors have been proposed as reference design connectors:
1. 44-pin PCB-mount DB receptacle (section 3.1.1)
2. 44-pin PCB-mount DB plug (section 3.3.1)
3. 44-pin Bulkhead Direct Attached receptacle (section 3.1.2)
4. 26-pin cable-mount signal receptacle (section 3.1.3) and PCB-mount plug (section 3.1.4)
5. 6-pin DB Host Power header (section 3.1.6.1) and receptacle (section 3.1.7)

Part drawings and footprints for some of these connectors are provided for reference design purposes. Detail dimensions, footprints, cable lengths/types, performance data, etc. should be consulted with and acquired from corresponding part manufacturers.

4. Enclosures

The DB spec. defined only the three device form factors – DB13, DB20 and DB32 – as the "interface" between devices and systems for Device Bay applications. Based on these device form factors a system manufacturer can extrapolate the enclosure designs to accommodate different types and numbers of devices. The DB spec. did not define the bay enclosures to give more freedom to the system manufacturers. Example areas are the bay openings, slide trays, the locking mechanism, the receptacle connector types and the user-interfaces (e.g., removal push buttons and displays). There are just too many variations on the system implementation choices, considering the types and number of devices to be supported, and the overall system form factor, such as desktop, tower, portables, etc.

This section is to give a few examples as an introductory to Device Bay implementation. It is a sole responsibility for a system or a device manufacturer to do the diligence such as cost/performance trade-off and to meet its respective customers' requirements. Though the system examples are computer applications, the concept can be applied to other types of systems, such as consumer electronic, test/measurement, data acquisition, etc.

The hope is to enable generic bay cages and device shells along with various hardware choices such as locking features, interconnectivity and user-interface buttons/displays.

4.1. Integrated Bay Cages

An "integrated bay" is a bay inside a computer chassis. The Device Bay Controller (DBC) can be ACPI- or USB-based. There should be enough number of 1394 and the USB ports inside the system to support the maximum number of bays to be supported. The power supply also has to be able to support the maximum number of bays. The bay receptacles can be of either PCB- or cable-mount type (see Section 2.1 for interconnectivity).

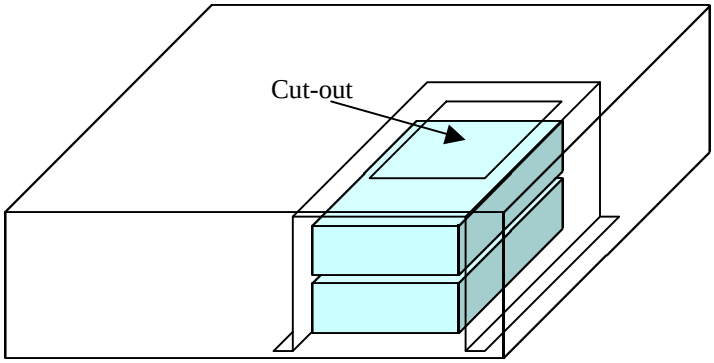


Figure 37. An integrated two-bay Device Bay desktop system example.

The DB bay cage can be implemented in such a way that the locking/ejection mechanisms are directly attached to the cage itself. In today's standard PC chassis form factors, a 2-bay cage can fit within the 5¼"drive bay volume area. The space on the sides of the bay cage is less restrictive for a desktop compared to a tower form factor. Similarly, the space on the rear of the bay cage is less restrictive for a tower compared to a desktop form factor. Therefore, if solenoids are to be used for ejection mechanism then they can be mounted on the sides for a desktop cage and on the rear for a tower cage. [**Tip:** A rectangular cut-out on the top of the bay cage (sheet metal) can be useful for inspection or servicing the bay mechanisms as shown in Figure 37. It is almost a requirement if a bulkhead connector is to be mounted from the front side of the bay.]

4.2. Remote Bay Cages

A “remote bay” is a bay that is totally separated from a computer chassis. A vertically-stacked remote bay is also

A remote condo is an independent subsystem that can be used with various types of host systems. A host system can support one or many remote condos, limited by the number of devices supported by USB and/or 1394 architecture. Remote condos are very effective for applications such as,

- peripheral expansion for a laptop,
- server disk arrays,
- gang-programming station for mass storage,
- entertainment system “component rack,”
- industrial control modules,
- test/measurement modules, and
- data acquisition modules.

For a remote bay, the DBC has to be USB-based and the remote condo’s USB port interfaces to one of the USB walkup connectors on a computer. There should be enough number of 1394 and the USB ports inside a remote condo to support the maximum number of bays to be supported. The power supply in a remote condo also has to be able to support the maximum number of bays. The bay receptacles can be of either PCB- or cable-mount type (see Section 2.2 for the interconnectivity).

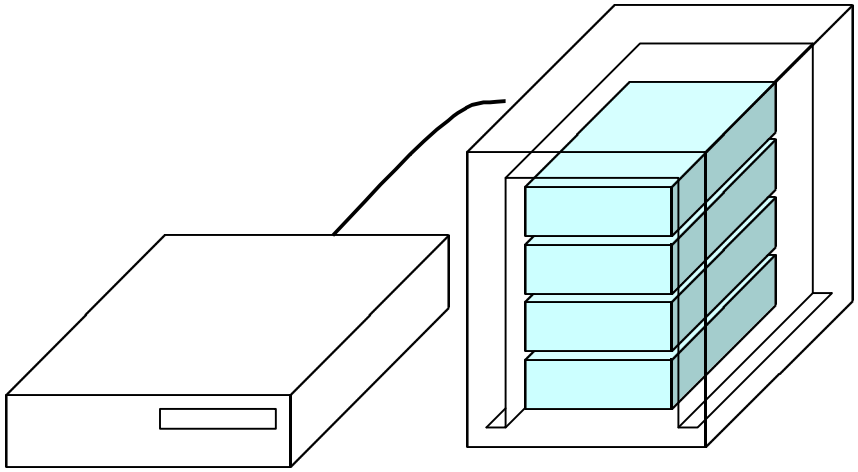


Figure 38. A remote four-bay Device Bay “condo” example.

4.3. Device Shells

The external form factor features of a device enclosure are defined in the Device Bay Interface Specification. The internal features of a device enclosure can be of any design. The followings are suggestions for those enclosure manufacturers who wish to offer generic enclosures for Device Bay applications:

1. LD Shell -- to hold "legacy" devices and necessary interface electronics
2. AD Shell – to mechanically adapt smaller form factor Device Bay devices to a larger form-factor, e.g., DA32 Shell to adapt DB13 and DB20 devices to a DB32 bay.

4.3.1. Legacy Device (LD) Shell

A LD shell is to accept existing devices with different form factors by means of "personalized" internal brackets that can be mounted the same way. Example existing devices are as follow:

- standard 3.5" devices
- system OEM specific portable devices

Most of these devices have IDE interface. An adapter board to translate from the 1394 to IDE needs to be mounted somehow within a LD shell. The size, the shape and the mounting of the adapter board inside a LD shell may vary depending on the form factor of an existing device. For example, the adapter board may be situated horizontally (as shown in Figure 39) or vertically.

A generic Legacy Device Shell should have the following features as standard (for a vendor):

- mounting feature dimensions for the personalized brackets
- mounting feature dimensions for the adapter board

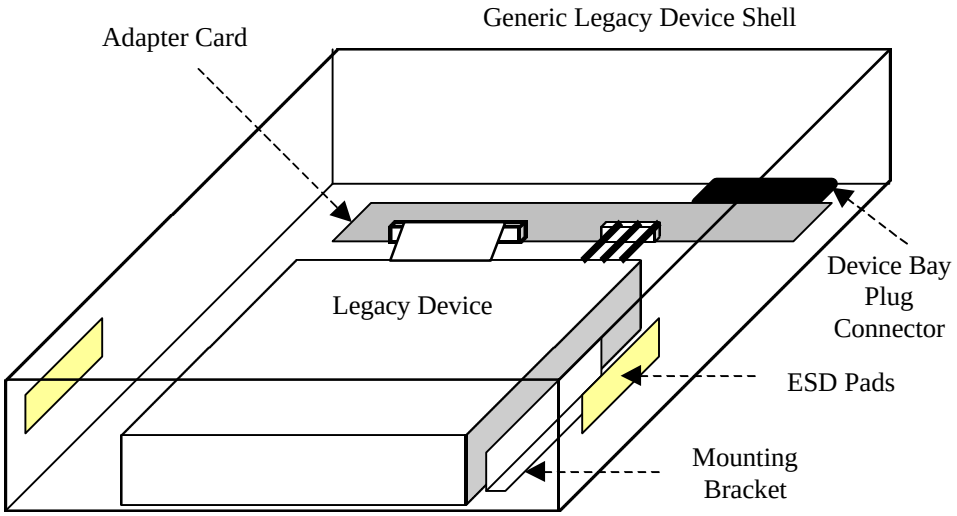


Figure 39. A generic Legacy Device Shell example.

4.3.2. Adapter (AD) Shell

A generic adapter shell is to use a smaller, i.e., DB13 or DB20, device in a DB32 bay. If the smaller device does not require a front access, e.g., a hard disk drive, a cable modem, then the adapter will be a simple form factor adapter shell. Figure 40 shows a over-simplified version where there are no connectors within the adapter itself. The bay receptacle will mate directly to the device plug mounted inside the smaller device. It is important to note that the ESD pads of the smaller device need to be somehow connected to the ESD pads of the adapter shell.

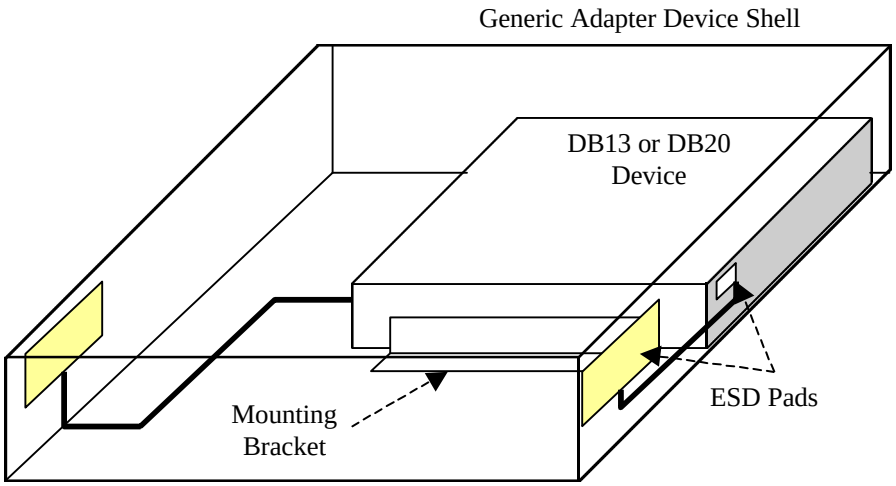


Figure 40. A generic Adapter DB32 Device Shell for smaller DB devices that do not require front access.

If the smaller device requires a front access, e.g., a CD-ROM, ZIP drive, then the adapter will need to have an adapter card to interface between the plug in the smaller and the plug to be mated to the bay receptacle (Figure 41 shows a over-simplified version). It is important to note that the ESD pads of the smaller device need to be somehow connected to the ESD pads of the adapter shell.

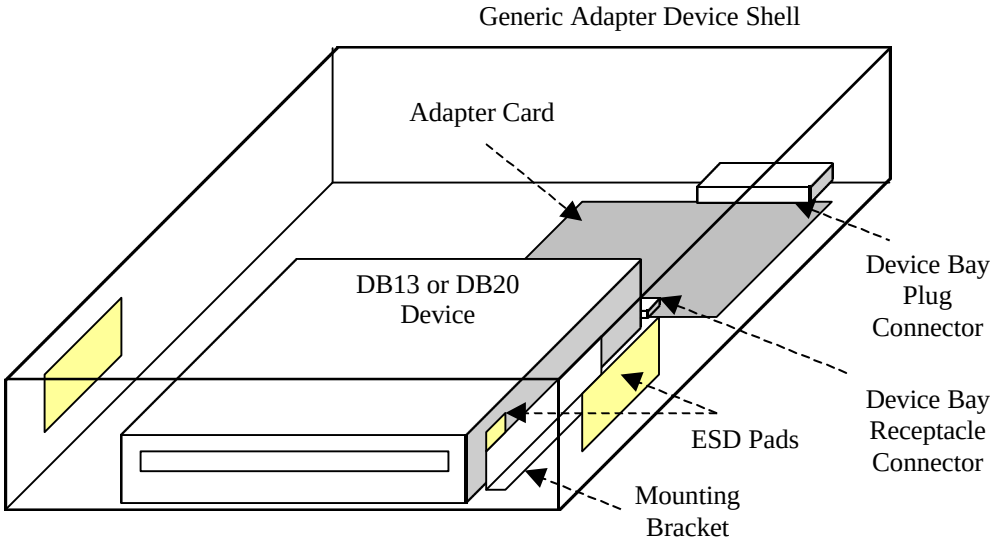


Figure 41. A generic Adapter DB32 device shell for front-accessible smaller DB devices.

5. Device Bay Power Control Design guide

5.1. Background

The purpose of this section is to provide the Device Bay (DB) device and bay designers with a starting point for their design. It is NOT meant to replace the engineering that must be done to have a completely DB compliant and functional system design.

DB power control is not a hot-plug from the "physical" sense. However, from an engineering point of view its close enough.

a) V_{id} is required to be off when a device is inserted in the bay.
b) V_{op} may or may not be hot when the device is inserted
c) The device is not allowed to draw any more than 5μA until it is authorized.
d) V_{op} authorization arrives well after V_{id} is enabled.
e) V_{id} is required to be off when a device is removed from the bay.
f) A software controlled interlock is REQUIRED – No surprise removals are allowed.
g) When V_{id} is enabled, it will be turned on in such a way as to not disturb the rest of the system power.
h) When power is enabled (i.e., to be drawn off V_{op}), the device will do so in away that does not disturb the other devices' power and the system power.

Power control for V_{op} was placed in the device for many reasons. Several of them are listed as follow:

a) The device knows and only controls the power rails it needs.
b) The device knows how much power it will consume and can scale its power control appropriately.
c) Once enabled, the device uses the native bus (1394 or USB) ACPI power control of the DB subsystem.
d) The device knows its di/dt requirements and can size its local bulk capacitance appropriately.

5.1.1. Measurement and Specification

All DB power measurements and specifications are to be verified at the following location:

- For the bay: At the contact in the receptacle connector
- For the device: At the contact in the plug connector

These where chosen for the following reasons:

1. The bay and the device must have a specification point that is with in their control to meet and use the specification.
2. The bay is not responsible for maintaining compliance with the device past the mating section of the DB connector. If the device wants to use a 200Ω connector and a 200Ω power control device, it is not the bay that will not be compliant if such a device does not work. It is the responsibility of the device to use a compliant connector and to use appropriate power control devices.
3. The device is not responsible for the components in the bay. The bay must provide the required power levels regardless if it has power control devices in line or not, the device can and must demand compliant power levels to be delivered to the device's DB plug connector.

The transient current limits in the DB spec. are intended to be absolute maximums.

The followings are four interesting power measurement points in time for a DB device:

1. **Device insertion into the bay, with the V_{op} hot.**
   a) Of interest is the transients that are created which can be caused by the input capacitance of the device and its power control circuitry.
   b) Also of interest is the ability of the device to keep its V_{op} power control circuits off even when no power is being applied to the control input.

2. **When V_{id} is enabled.**
   a) There is some challenge to keep the power control input glitch free and off while the power is being enabled to the controlling device.

3. **When V_{op} is enabled.**
   a) For a 1394 storage device, it is caused by the Login-Command and for a USB device it is signified by the End-Configuration.
   b) Of interest if the following:
      I. Inrush current on all three V_{op} voltage rails, absolute maximum, peak and maximum di/dt.
      II. Voltage levels in the system at each of the voltage rails (3.3V, 5V and 12V)

4. **Operational time.**
   a) The device must meet all the worst-case Di/dt requirements defined in the DB spec.

A device must meet or be below the maximum current ratings and rate of current change as outlined in the Device Bay spec under all four of the conditions outlined above.

5.1.2. Device Bay Power Type

Device Bay power is considered to be:
1. Separate from the cable power of each of the (1394 and USB) native busses.
2. Internal system power. Analogous to today's 5V/12V 4-pin PC power connector. For safety reasons the receptacle is in the bay. For protection (both mechanical and electrical), the plug connector in a device is recessed (2.0mm for a DB32 form-factor).
3. Controlled by a separate power manager from the Native bus power managers.

The USB/1394 walkup cable power pins are not present on the DB bay connector, as the DB connectors support only the differential signals and their protocols for USB and 1394.

If a device provides an externally accessible (1394 and/or USB) native bus connector, it must provide all the required power protection for an external connection and must assume the bay will provide absolutely no protection at all. This includes both signal and power protection.

5.2. Bay Power Delivery and Control

5.2.1. V_{id} Bay-Side Power

While Vid is 3.3V it will not be a feed back controlled output of the power supply. This means V_{id} will rise and fall with the power requirements and losses off the feed back voltage (if there is one, usually 3.3V because that is what the Voltage Regulation Module, VRM, for the processor uses). Given the system holds a ±5% 3.3V tolerance to the VRM, the voltage to the input of the FET could have a much higher variance. To satisfy the ±5% tolerance on V_{id} the system will mostly likely have to regulate the 3.3V to ±2%, and allocate an additional 1% since V_{id} is not the control voltage, for a total tolerance of ±3% at the input to the FET. This allows the Bay designer 2% for the V_{id} insertion losses.

From the DB spec.:
a) Maximum current for V_{id} is (1.5W / 3.3V) = 0.454A.
b) Maximum voltage insertion loss = 3.3V * 0.02 = 0.066V.
c) Maximum V_{id} Insertion resistance = 0.066V / 0.454A = 0.1454Ω (145mΩ)

5.2.1.1 V_{id} Bay-Side Power Delivery

A typical system may have several connectors in line with 3.3V:
a) Power supply connection to the system board. (This connector's insertion loss *may* be removed if the system uses a sense lead).
b) If the system is a NLX type chassis there will be another connector between the riser card and the system board. (Again the connector's insertion loss *may* be removed if the system uses a sense lead).
c) If the V_{id} FET is on the system board for a NLX chassis, V_{id} will have riser card as source of insertion loss.
d) System board or riser card V_{id} connector.
e) Termination for the DB bay receptacle, which could be, in of increasing resistance, solder, crimp or IDC.

5.2.1.2 V_{id} Bay-Side Power Control

In order not to violate the V_{id} spec to other DB devices or other devices in the system, the bay is required to have some type of edge rate (Di/dt) control when it enabled V_{id}.

5.2.1.3 V_{id} Bay-Side Insertion Loss

The followings are many sources of insertion loss and many are dependent on the system design:
a) **[System Design Dependent]** Power regulation of 3.3V at the input of the V_{id} FET. If V_{id} is powered off of the Vaux power supply to support wake-up events, the system may have another FET in-line to switch V_{id} from main 3.3V power to Vaux33.
b) **[System Design Dependent]** Size of the V_{id} FET.
c) **[System Design Dependent]** Size of the wire to connector the V_{id} FET to the DB bay receptacle.
d) **[System Design Dependent]** Length of the wire to connect the V_{id} FET to the DB bay receptacle.
e) **[System Design Dependent]** Type of connection used to connect V_{id} (solid vs. stranded vs. PCB trace).
f) **[System Design Dependent]** Choice of how V_{id} wire connects to the FET (power connector, DB signal connector).
g) **[System Design Dependent]** Choice of what type of DB bay receptacle is used and therefor the type of connection the V_{id} wire has to the backside of the DB bay receptacle (solder, crimp, IDC).
h) **[DB spec.]** Maximum current is fixed in the spec at 0.454A.
i) **[DB spec.]** Maximum voltage tolerance at the DB bay receptacle.

Vid Current (Amps) =	0.4540		
PCB DB conn. LLCR (Ohms) =	0.0300		
Device DB conn. LLCR (Ohms) =	0.0300		
FET trench resistance (Ohms) =	0.0300		
Cable length (inches) =	16		
Wire AWG (7-strands) =	**28**	**26**	**24**
Wire resistance (Ohms)/ft =	0.0620	0.0391	0.0239
Cable resistance (Ohms) =	0.0827	0.0521	0.0319
Total Vid path resistance =	**0.1727**	**0.1421**	**0.1219**
Vid (V) => **3.30**			
24AWG 1.68%			
26AWG 1.96%			
28AWG 2.38%			

Figure 42 - V_{id} Insertion Loss spreadsheet

5.2.2. V_{op} Bay-Side Power

5.2.2.1 V_{op} Bay-Side Power Delivery

The bay side should have a local source of electrons (capacitors) on each of the Vop power rails.

Vop (3.3V)

- Should use two 18AWG wires to reduce insertion loss and handle the total current.
- Uses six contacts on DB bay receptacle (effective LLCR resistance = 0.030/6 = 0.005Ω).
- Needs to support 5.25A Peak and maintain a valid voltage level.

V_{op} (5V)

- Should use one 18AWG wire.
- Uses three contacts on DB bay receptacle (effective LLCR resistance = 0.030/3 = 0.010 Ω).
- Needs to support 3A peak and maintain a valid voltage level.

V_{op} (12)

- Should use one 18AWG wire.
- Uses three contacts on DB bay receptacle (effective LLCR resistance = 0.030/3 = 0.010Ω).
- Needs to support 3.75A Peak and maintain a valid voltage level.

V_{op} (GND)

- Should use two 18AWG wires.
- Uses six contacts on DB bay receptacle (effective LLCR resistance = 0.030/6 = 0.005Ω)
- Needs to support (just) about 6A Peak and keep a valid ground reference.

5.2.2.2 V_{op} Bay-Side Power Control

Optional – For 3.3V, at 5.25A this would require a 0.01257 ohm FET to only drop 2% (3.3V * 0.02) / 5.25A
This is a absolute worst-case number across full process, temperature, thus would require a < 0.007Ω typical FET.

5.2.2.3 V_{op} Bay-Side Insertion Loss

V_{op} (3.3V) – budget 2%
V_{op} (5V) – budget 2%
V_{op} (12V) – budget 3%

5.3. Device Power Delivery and Control

5.3.1. V_{id} Device-Side Power

5.3.1.1 V_{id} Device-Side Power Delivery

The device is required to connect to all ground pins on the DB plug connector (both signal and power grounds), even if the device is fully powered off of V_{id}. This is done to decrease the ground rise due to IR loss on the ground.

5.3.1.2 V_{id} Device-Side Power Control

There is no V_{id} power control envisioned (optional or required) on the device side.

5.3.1.3 V_{id} Device-Side Insertion Loss

Sources of V_{id} device side insertion loss includes:

1) Device side connector losses. Different connectors will have different connectivity to the PCB and thus will have different resistance.
2) Trace routing from V_{id} to each of the devices. In general a number of devices will need to be powered off of V_{id} so keep those traces short and wide. 0.454A is a lot of current for a standard 6mil signal trace.
3) Lack of termination of the ground pins in the V_{op} side of the connector can increase the IR losses on the return path back to the system. Termination of the V_{op} grounds is required if the device uses any of the V_{op} power, but optional the device only uses V_{id}.

5.3.2. V_{op} Device-Side Power

Because of how the power is regulated in a PC, today's devices (HDD, CD-ROM etc) do not get 5% regulation on 5V, or 10% on 12V. Many PC power supplies have no active voltage control feedback (sense) and if they do it comes from the processor area. Most of the power supplies don't even spec the power to the drive connectors and if they do they either need to pad it to compensate or the specification is not accurate.

The DB spec has changed the regulation requirement on both the V_{op}33V and V_{op}5V rails from ±5% to +5%/-3% to allow for the insertion loss of the V_{op} power control on the device.

5.3.2.1 V_{op} Device-Side Power Delivery

TBD

5.3.2.2 V_{op} Device side power control

Several items to watch out for:

- Input current of the power control devices.
- Pull-up and Pull-downs between the connector and the power switches.
- Power up race conditions. Including glitch free during device insertion, V_{id} turn-on and V_{op} enabling.

5.3.2.3 V_{op} Device-Side Insertion Loss

TBD

5.4. Device Bay Power Control Examples

5.4.1. Unitrode

Unitrode's DB power control example features:

- User-programmable closed-loop inrush current slew-rate limiting
- Individual low leakage shut down function
- User-programmable maximum current limit
- Internal charge pump to drive external low Rds(ON) N-channel MOSFETs
- Short-circuit protection and fault indication

5.4.1.1 Circuit Design Summary

Device-side (V_{op}) and bay-side (V_{id}) power rails are controlled using individual Hot Swap Power Managers (HSPM). The use of individual HSPMs provides the designer with increased flexibility in component placement and board layout while maintaining a maximum level of fault protection. Independent shutdown functions allow the power rails to be individually disabled or sequenced in a particular order. The HSPMs used in this reference design have internal charge pumps to drive the external N-channel MOSFETs. The following is a brief summary of the features and operation of the UCC3919 and UC3914 Hot Swap Power Managers used in the DB reference design. Please refer to www.unitrode.com/device-bay for more detailed design information.

5.4.1.2 5V and 3.3V V_{op} Device-Side and 3.3V V_{id} Bay-Side Power Control

The device-side 5V and 3.3V V_{op} power rails are controlled using UCC3919 Hot Swap Power Managers. The UCC3919 utilizes an on-board Linear Current Amplifier (LCA) to provide the user with direct, closed-loop control over the startup current profile regardless of MOSFET parametric variances or variations in load capacitance. The LCA can be programmed to meet generic Di/dt requirements or customized to meet specific device load requirements. The HSPM controls the current startup profile by actively limiting the amount of current (I_{MAX}) that the MOSFET can source to the load. The startup current profile is easily programmed through a RC network at the IMAX pin. An internal reference voltage (referenced to VCC) is provided to eliminate the effect of variances in VCC on the current limit.

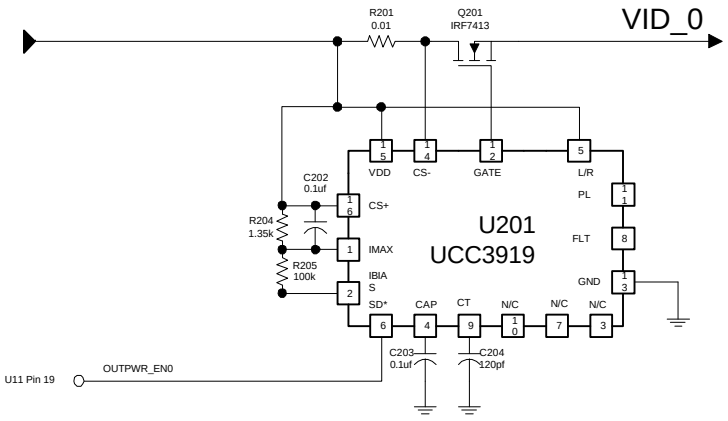


Figure 43 – Bay-side V_{id} hot-swap control

In addition to allowing the designer to customize the current profile during startup, the UCC3919 also provides several levels of fault protection and modes of fault handling as well as a fault output indicator pin. The UCC3919 may be programmed for manual or automatic retry modes during a fault condition. For the DB reference design, the manual (latched) mode of fault operation was selected. In the manual mode the MOSFET will latch off and remain OFF until either the input power is removed or the L/R pin is pulled toggled. The automatic retry mode or hiccup mode operates on approximately a 3% duty cycle, periodically turning on the output to detect if the fault is still present. During the ON time the output current will be limited to the user-programmed value of IMAX. If the fault has been removed before the MOSFET turns on again, the MOSFET will remain on. If the fault is still present the IC will reinitiate the fault sequence.

Short-circuit protection is also provided. Load currents greater than (200mv/RSENSE) +IMAX will trigger an internal comparator that will immediately shut down the external MOSFET. A second current detection threshold is Ifault. The Ifault threshold is set lower than the IMAX threshold but above the normal steady state load current. Ifault is used to detect prolonged periods of an over current condition.

5.4.1.3 12V V_{op} Device-Side Power

The device-side 12V V_{op} power rail is controlled using the UC3914 HSPM. The UC3914 was chosen because of its operating voltage range. Like the UCC3919, the UC3914 operation is based around a Linear Current Amplifier to provide closed loop control of the output current. Fault detection and handling are compatible with the UCC3919. Detailed information on the operation of the UCC3914 can be found on the Unitrode web site at www.unitrode.com. Transistors Q402, Q403, and Q406 are required to meet the shutdown leakage requirement (5µA) of the DB spec. Unitrode is committed to developing and producing HSPMs that provide ease of design compliance to the DB spec. with minimal external parts count.

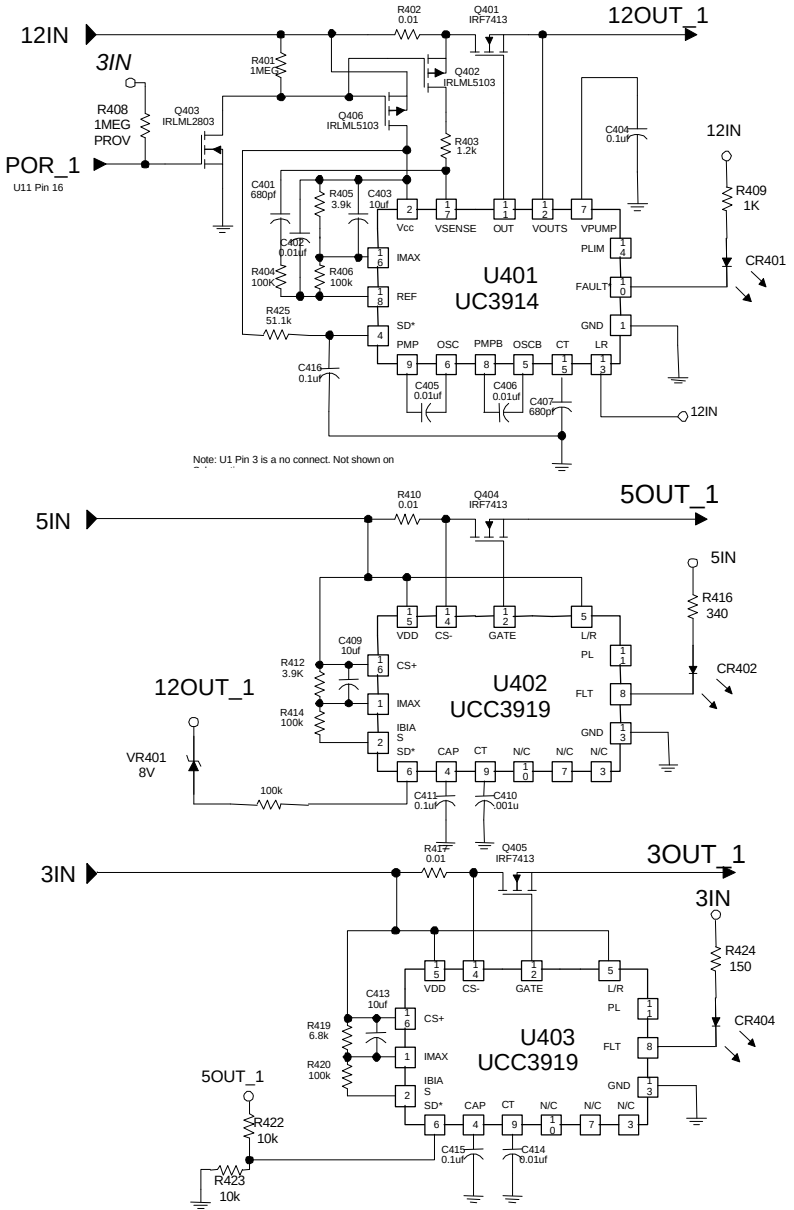


Figure 44 – Device-side V_{op} hot-swap power control

6. Electrical Performance for Signals

The electrical performance for signals of Device Bay related connectors and cable assemblies is characterized with the following parameters:

- Differential Impedance
- Differential Crosstalk
- Insertion Loss
- Signal Skew
- Propagation Delay
- EMI

See [5] for detail measurements and analyses on these parameters. A summary of the information in [5] will be eventually incorporated in this section.

6.1. Electrical Performance Parameters

6.1.1. Differential Impedance

TBD

6.1.2. Insertion Loss

TBD

6.1.3. Differential Crosstalk

TBD

6.1.4. Signal Skew

TBD

6.1.5. Propagation Delay

TBD

6.1.6. EMI

TBD

6.2. Electrical Performance Measurements and Validation Recommendations

This section describes how to verify the signal quality on both the host and the device sides by using an example host and device implementation.

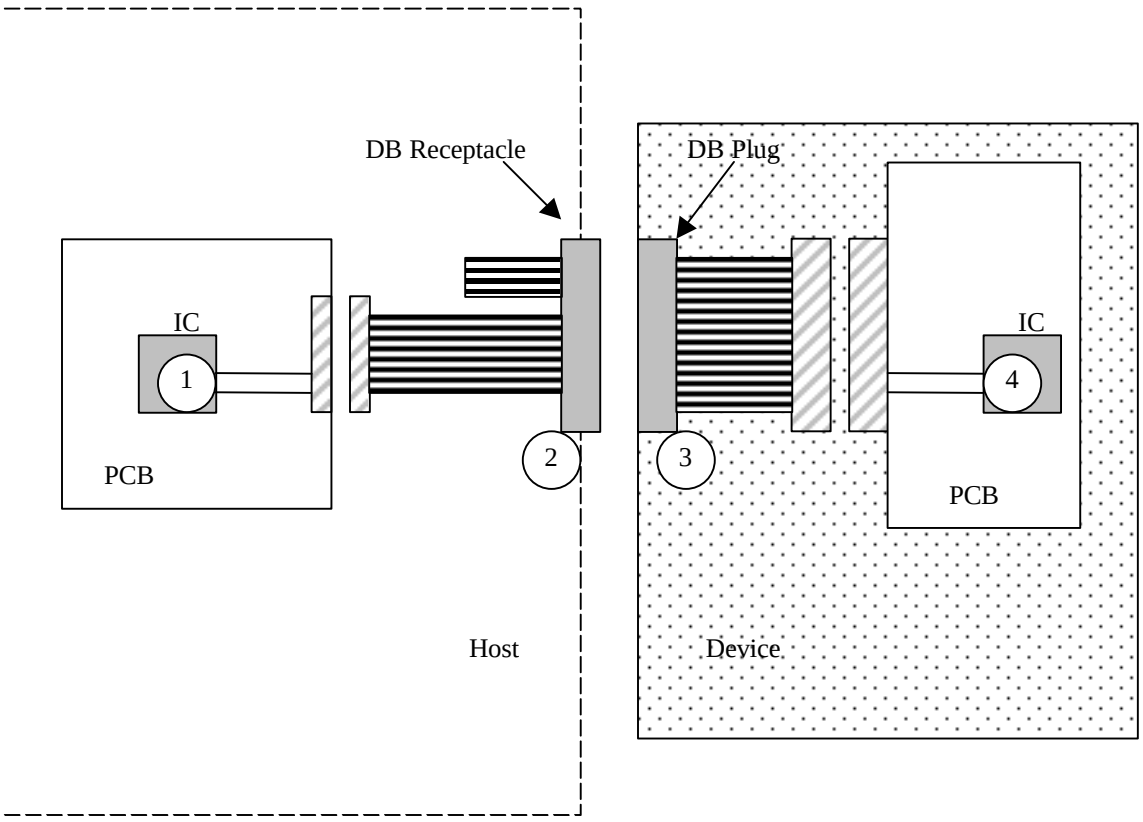


Figure 45. Example end-to-end connectivity chain for a Device Bay signal.

The following test points (TP) will be used in the discussion:
1. Transmitter/receiver IC pin
2. DB receptacle tail pin in the bay
3. DB plug tail pin in a device [The “performance junction.”]
4. Receiver/Transmitter IC pin

For an implementation, they may be one ore more connector and/or cable assembly stages between the transmitter/receiver IC and a Device Bay connector. For illustrative purposes, we will assume that there is a stage of cable assembly between a Device Bay connector and the transmitter or receiver IC, in the host as well as in a device. The test procedure described below will illustrate how a system designer and a device designer could verify the system or the device side, respectively, without the knowledge of the other side. The only important point to make here is that the system side and the device side must provide a signal quality at the performance junction (TP3) as defined in the DB spec.

6.2.1. Host-Side Verification

Since any compliant device can be used in a Device Bay host, it is impossible for a system designer to know how the interconnectivity is going to be in a device. All a system designer can do is to comply with the DB spec. to provide the signal quality (TBD) at TP3. A test board with a surface-mount Device Bay plug and a number of SMA connectors can be used on the "Device Side" to measure the signal driven through the connectivity chain on the host side, as shown in Figure 46.

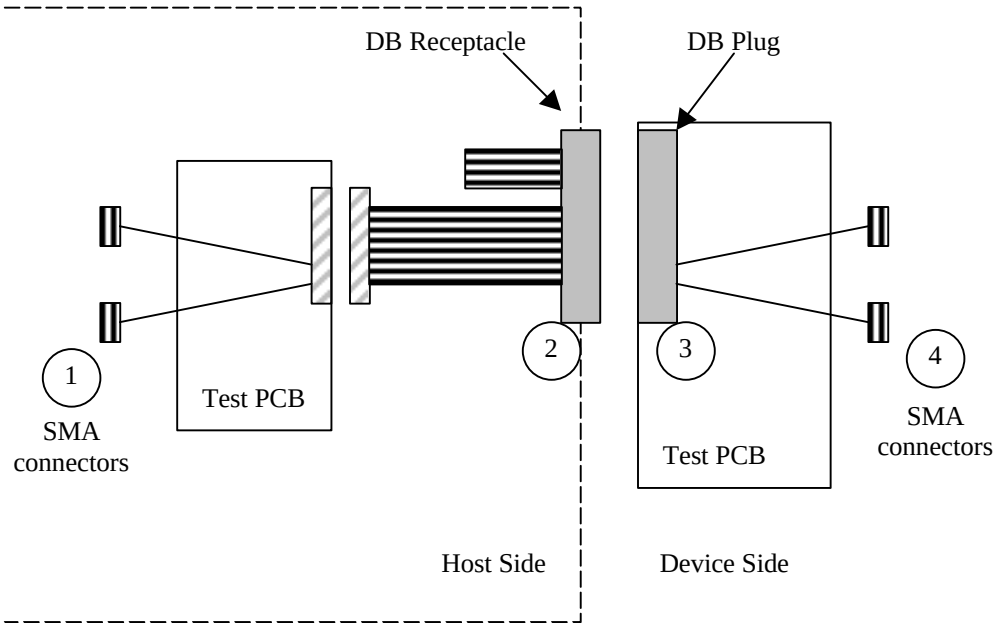


Figure 46. Host Under Test (HUT) example.

The measurement procedure is as follow:

1. Hook up a random pulse generator to one differential signal pin (e.g., A+) at TP1. Terminate a 50Ω resistor between the other differential signal pin (e.g., A-) and ground.
2. Hook up a digitizing oscilloscope is to one differential signal pin (e.g., A+) at TP4. Terminate a 50Ω resistor between the other differential signal pin (e.g., A-) and ground.
3. Connect the trigger output on the pulse generator and the trigger input on the oscilloscope.
4. The eye measured at TP4 should be within the sensitivity range defined in the 1394 spec. [3].

6.2.2. Device-Side Verification

Similar to Section 6.2.1, a device will likely be used in any DB compliant bay, it is impossible for a device designer to know how the interconnectivity is going to be in a system. All the device designer can do is to comply with the DB spec. to provide the signal quality (TBD) at TP3.

If it is not convenient to measure the differential signal quality at TP3 then perform the measuement at TP2 then prorate[12] the signal quality for TP3. A test board with a surface-mount Device Bay receptacle and a number of SMA connectors can be used on the "Host Side" to measure the signal driven through the connectivity chain on the device side, as shown in Figure 47.

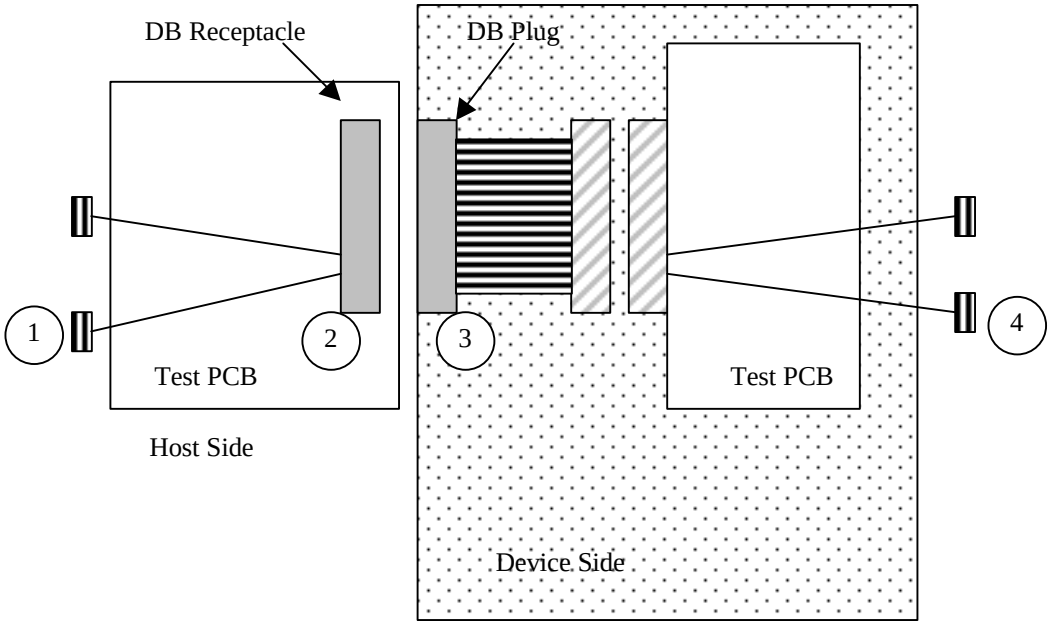


Figure 47. Device Under Test (DUT) example.

The measurement procedure is as follow:

1. Hook up a random pulse generator to one differential signal pin (e.g., A+) at TP4. Terminate a 50Ω resistor between the other differential signal pin (e.g., A-) and ground.
2. Hook up a digitizing oscilloscope is to one differential signal pin (e.g., A+) at TP1. Terminate a 50Ω resistor between the other differential signal pin (e.g., A-) and ground.
3. Connect the trigger output on the pulse generator and the trigger input on the oscilloscope.
4. The eye measured at TP1 should be within the sensitivity range defined in the 1394 spec. [3].

[12] Refer to any good microwave text book on "cascaded two port networks" on tips on how to prorate insertion losses.