High Speed Signal Processing

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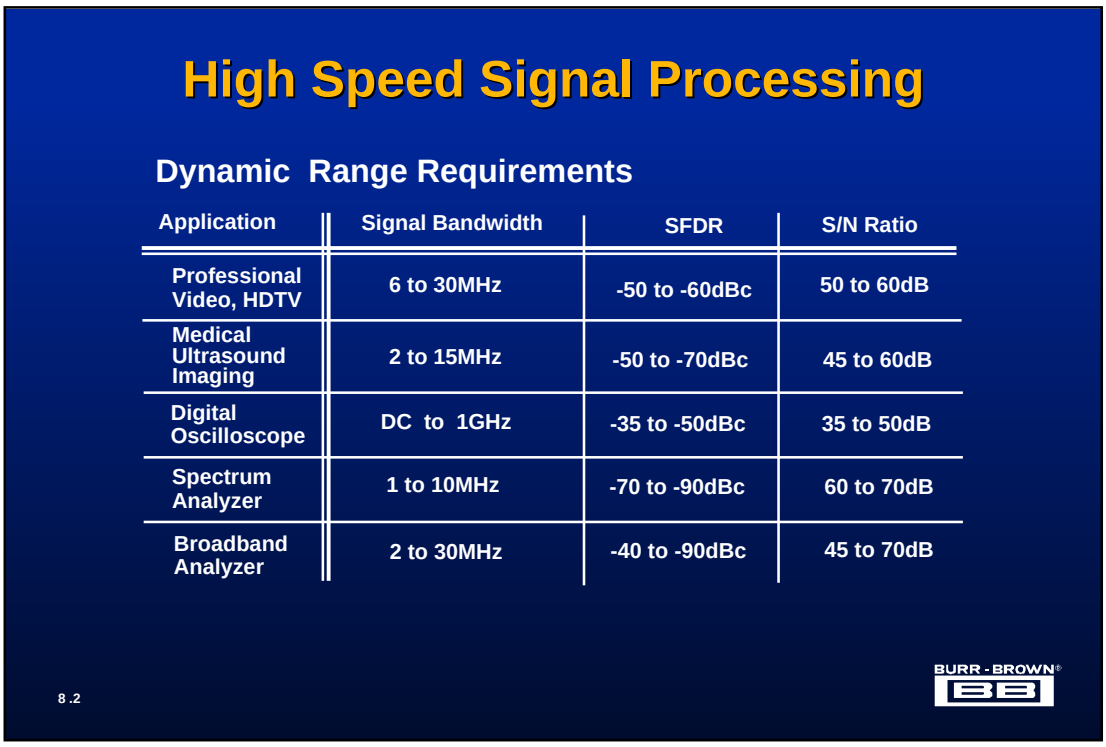
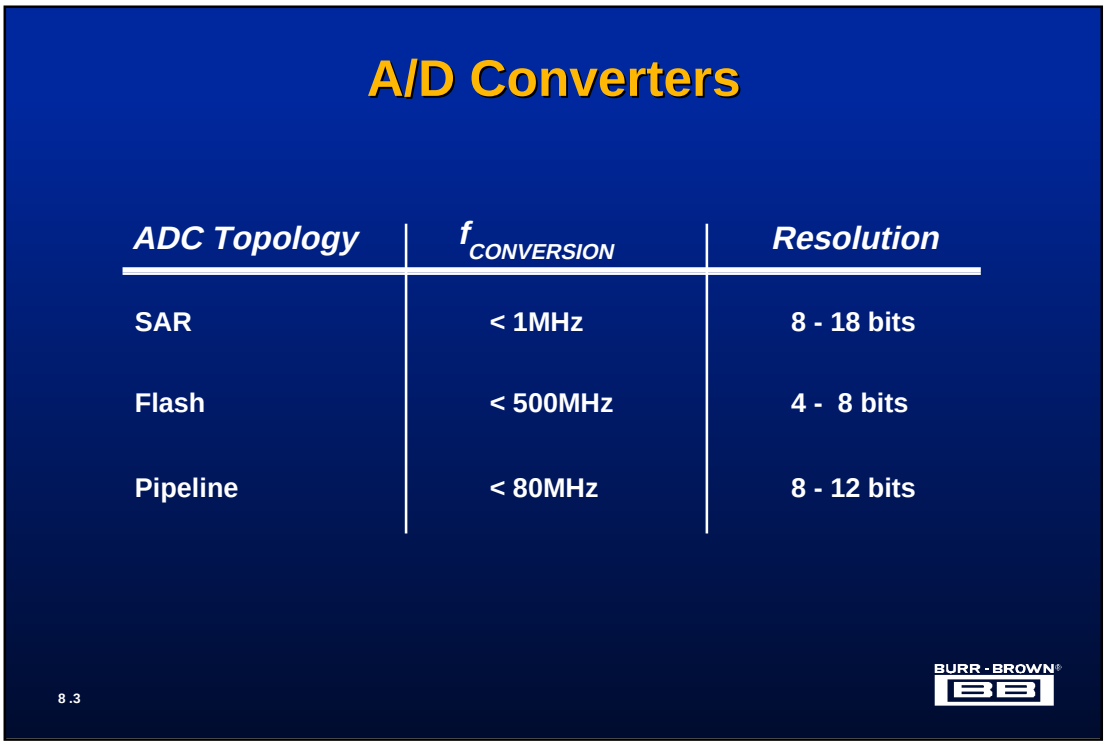


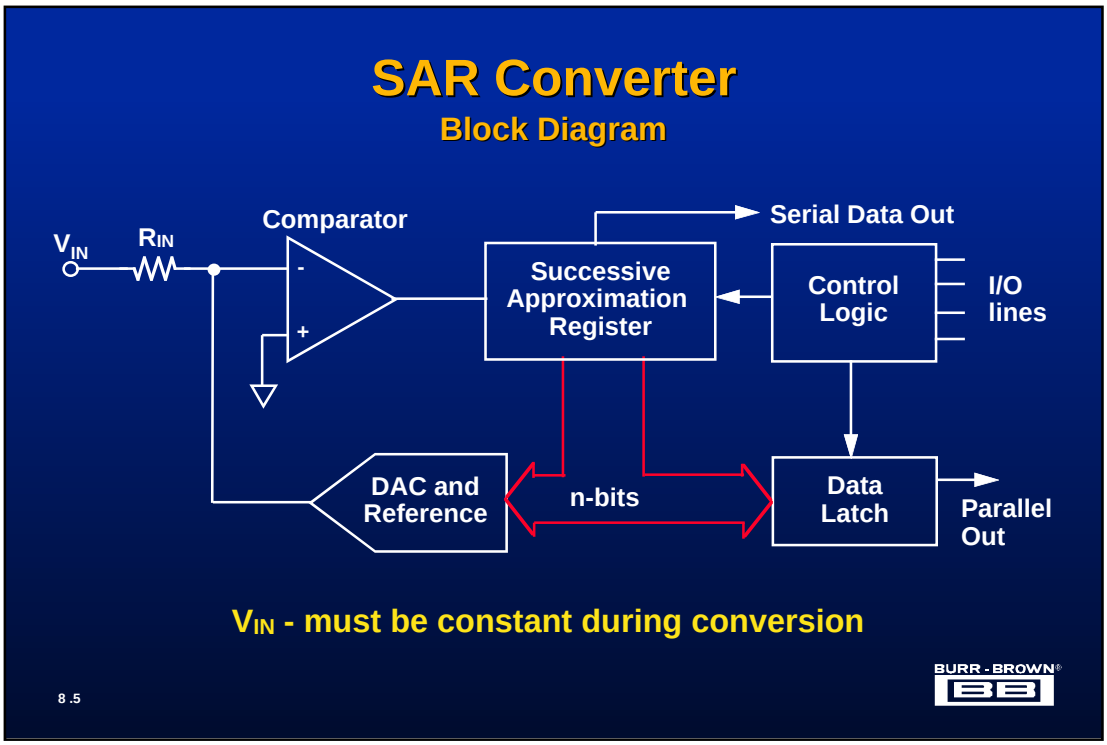
High Speed Signal Processing can infer a wide range of applications and frequency ranges. There are several classes of semiconductors that are used in the circuits for those applications. These classes can be categorized, according to the process used to manufacture the silicon. Burr-Brown has focused their efforts in high speed product development using silicon process rather than say Gallium type processes. The use of strictly silicon processes implies a certain complexity in the function and circuit bandwidth. Burr-Brown's high speed products find a home in applications such as professional video, medical ultrasound imagine, digital oscilloscopes, spectrum analyzers, and broadband analyzers, to name a few.



This section will compare the performance features and trade-offs of three different architectures found in high speed analog-to-digital converters. Each architecture has distinct characteristics that need to be properly understood to maximize the benefits of the chosen A/D converter with the individual application.

The three types of design that will be compared are the successive approximation (SAR), flash, and pipeline ADC. Each method of conversion has strengths and weaknesses, which will be contrasted throughout the discussion.

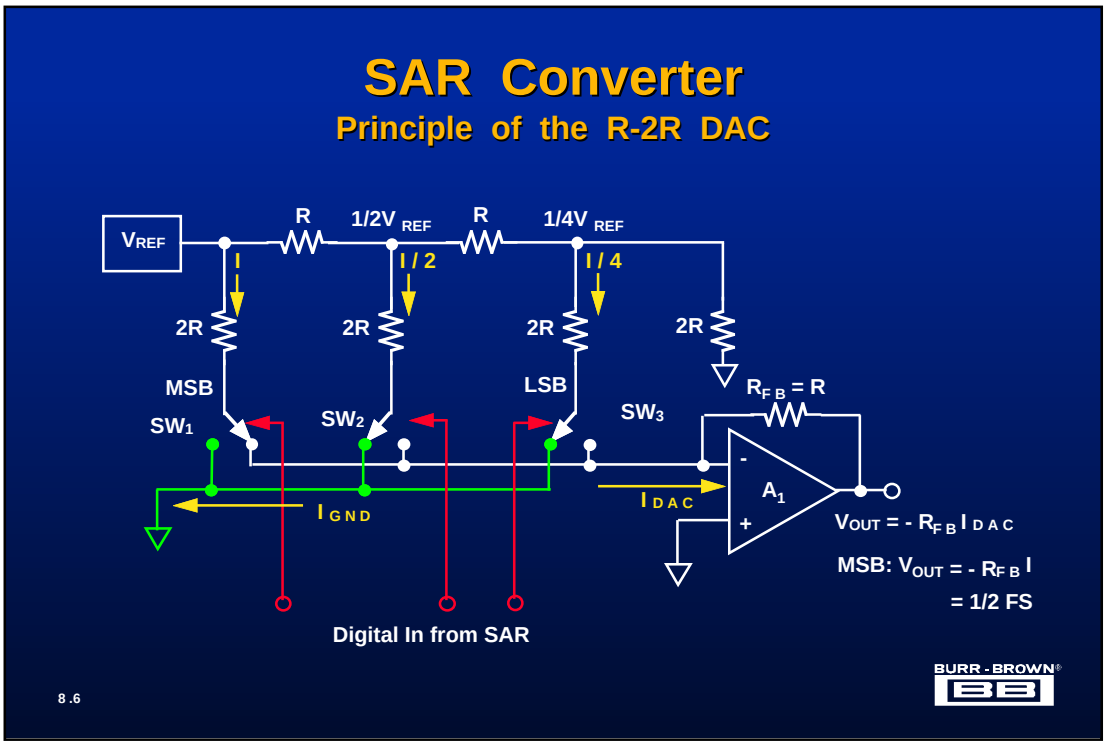
One of the most popular architectures that is employed for the design of analog-to-digital converters is “Successive Approximation”. One of the main reasons for this architecture’s success is its high degree of performance compared to its cost. Modern designs almost exclusively utilize new CMOS or BiCMOS processes which allow a reduction in chip size and power dissipation. Both of these features are important to a system user because lower power dissipation leads to a lower temperature rise, greater reliability, and fewer problems with warm-up and temperature drift. Also, it is possible to replace the well known R-2R ladder network with the so called CDAC. Instead of scaled resistors very stable capacitors are used, which implement a charge redistribution technique.



The block diagram of a typical Successive Approximation ADC is shown here. The circuit design is straightforward, employing only one single comparator along with a digital-to-analog converter and the successive approximation logic.

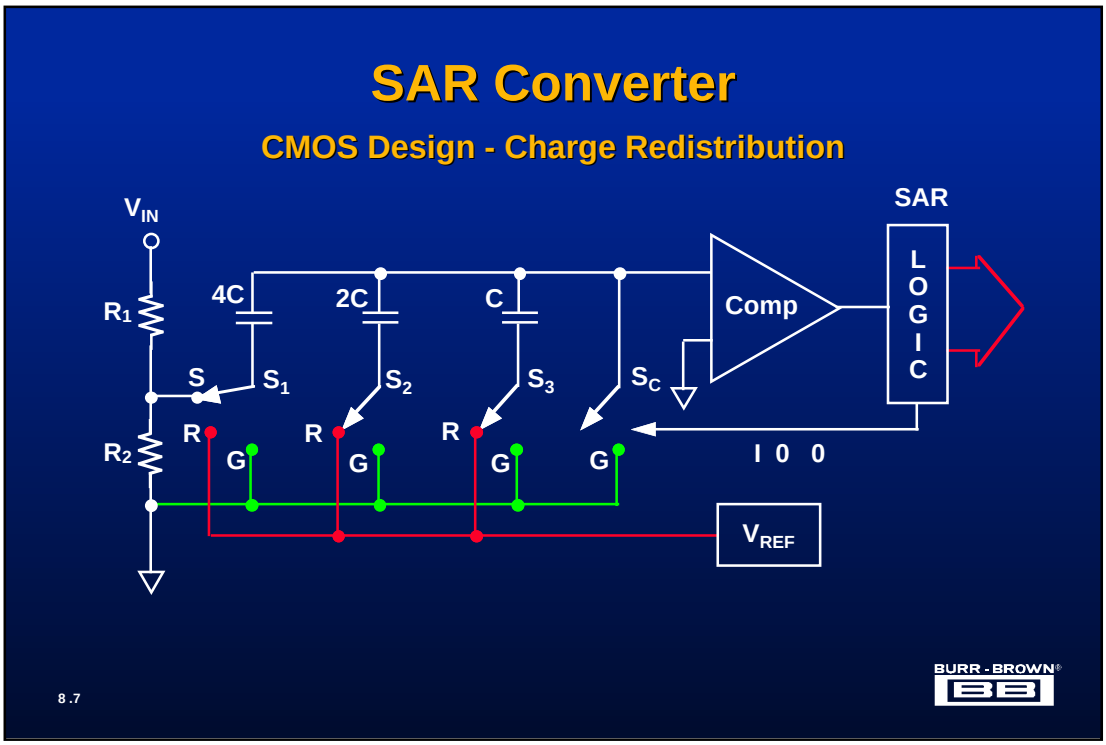
An analog signal of unknown magnitude is connected to one input of the comparator via the input resistor. Added to this signal is the output from the DAC. The successive approximation register provides the input to the DAC and responds to the output from the comparator. When the DAC has its MSB set to 1, with all other bits set to zero, the successive approximation register (SAR) will produce an output equivalent to half the reference voltage and analog input full-scale range. The comparator then determines if the DAC output is above or below the unknown input signal. If the input voltage is above the DAC output, the MSB is retained in the SAR while the next weight, fi the reference, is compared. This process continues until all bits are compared and the nearest approximation to the input signal is obtained. This result is then passed to the data latch.

This type of architecture requires the input signal to be held constant while the conversion process takes place. This limits the use of the SAR ADC to a very low frequency bandwidth, requiring a sample/hold circuit in front of the ADC. More recent SAR converter designs, using switched capacitor networks with charge redistribution, are replacing older resistive ladder DACs. The main advantages of the so called CDACs are the higher speeds, the inherent sample and hold function, the increased accuracy, and the smaller die size. The performance varies widely for designs employing this type of architecture, ranging from 8 to 18 bits of resolution with conversion rates from 50µs to about 1µs.



A simplified 3-bit version of the DAC inside a successive approximation A/D converter is shown here. It uses the R-2R ladder network to create the binary weighted currents which are constantly flowing through the shunt arms of the ladder.

The I_{DAC} and I_{GND} currents are maintained at ground potential, either by the op amp summing junction or by a direct connection to ground. The switches steer the current either to the summing junction or to ground depending on the individual digital logic levels applied to each of the switches coming from the SAR. For example, a logic 'high' to SW_1 will cause the current, I, of the most significant bit (MSB) to add to the I_{DAC}. For a digital 'low' the same current would flow to ground (I_{GND}). Since the magnitude of the MSB current is half of the full scale current it will result in an output voltage that is half of the full scale output voltage.

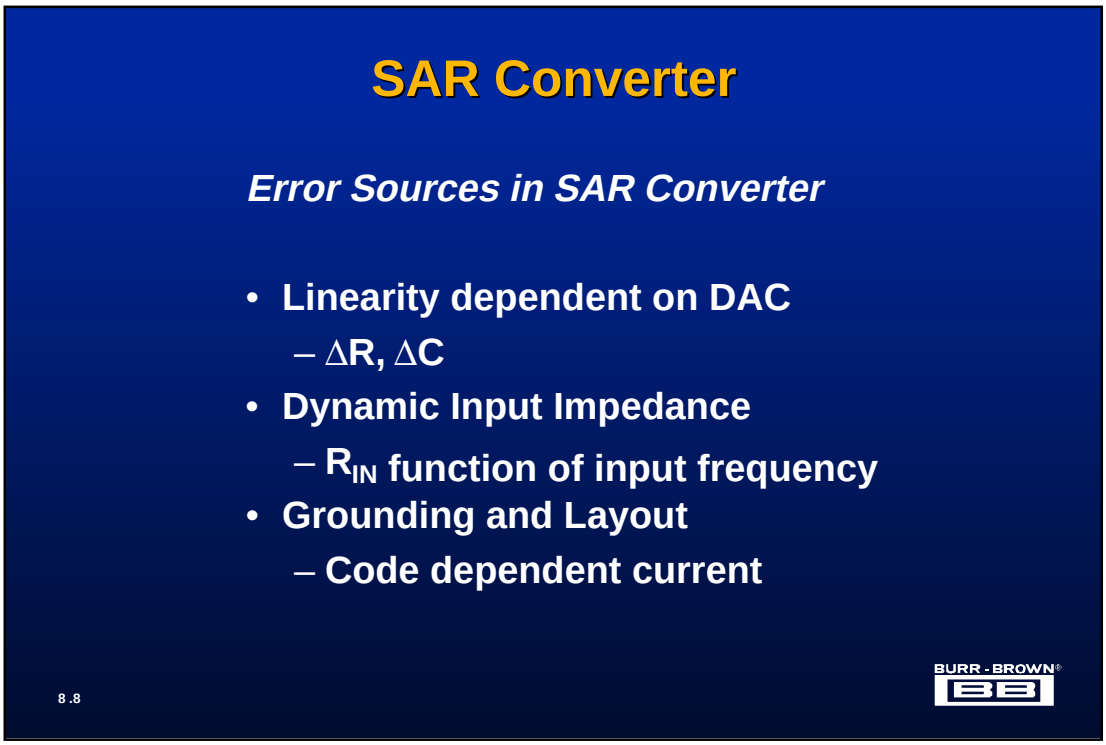


Instead of the previously discussed R-2R ladder, newer CMOS SAR converters use a charge redistribution scheme for the DAC block. For the propose of discussion, a simple 3-bit design is shown here. This CDAC approach has the added benefit of bringing the sampling mechanism inside the ADC package.

While in the sampling mode, the MSB switch (S_1) is in the “S” position, therefore the charge on the MSB capacitor is proportional to the voltage level of the analog input signal. The remaining switches (S_2 and S_3) are set to the “R” position to provide accurate bipolar offset from the reference source V_{REF}. At the same time switch (S_C) is also closed to ground to auto-zero any offset errors in the CMOS comparator.

A convert command will open switch S_1 to trap a charge on the MSB capacitor proportional to the input level at the time of the sampling command. Similarly, a charge is trapped on the rest of the array capacitors proportional to the reference voltage V_{REF}. The total charge trapped can now be moved between the three capacitors in the array by connecting switches S_1, S_2, and S_3 to position “R” or “G” successively, thereby changing the voltage seen at the comparator input.

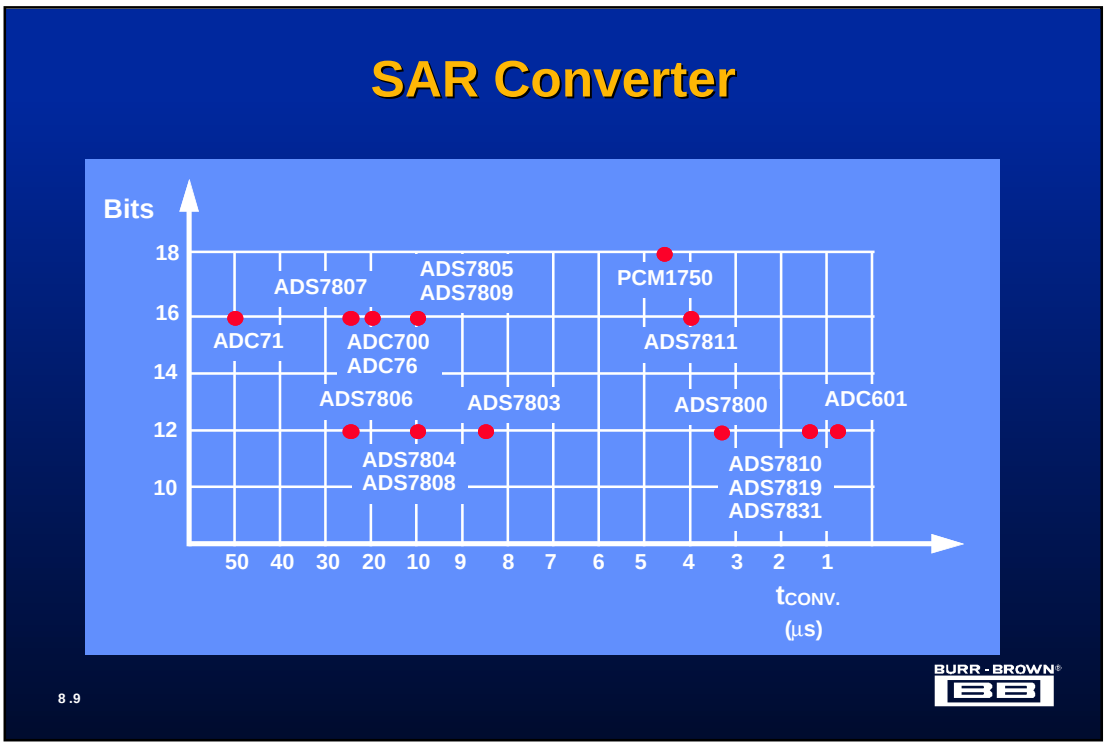
The first approximation connects the MSB capacitor via S_1 to V_{REF}, while switches S_2 and S_3 are connected to ground. Depending upon whether the comparator output is High or Low, the logic will then latch S_1 into the “R” or “G” position. Then the comparator moves on to make the next approximation by connecting S_2 to V_{REF} and S_3 to ground. When the three successive approximation steps are made, the voltage level at the comparator will be within 1/2LSB of ground level and the data output word will be based on reading the positions of S_1, S_2, and S_3.



The linearity of a successive approximation ADC depends on the linearity of the internal digital-to-analog converter, which is typically not true for other ADC architectures. With the SAR converter, the accuracy of the ladder resistors and their temperature coefficients affect the linearity errors and their variation with temperature. Added to these errors are the switch resistances (R_{ON}).

Furthermore, only the DAC has to settle to the final accuracy. This is not the case with a converter using the sub-ranging topology.

Older ADCs using the resistive R-2R ladder required special care for their layout, especially the routing of the analog and digital grounds, because they have a code dependent current flowing through the ground.

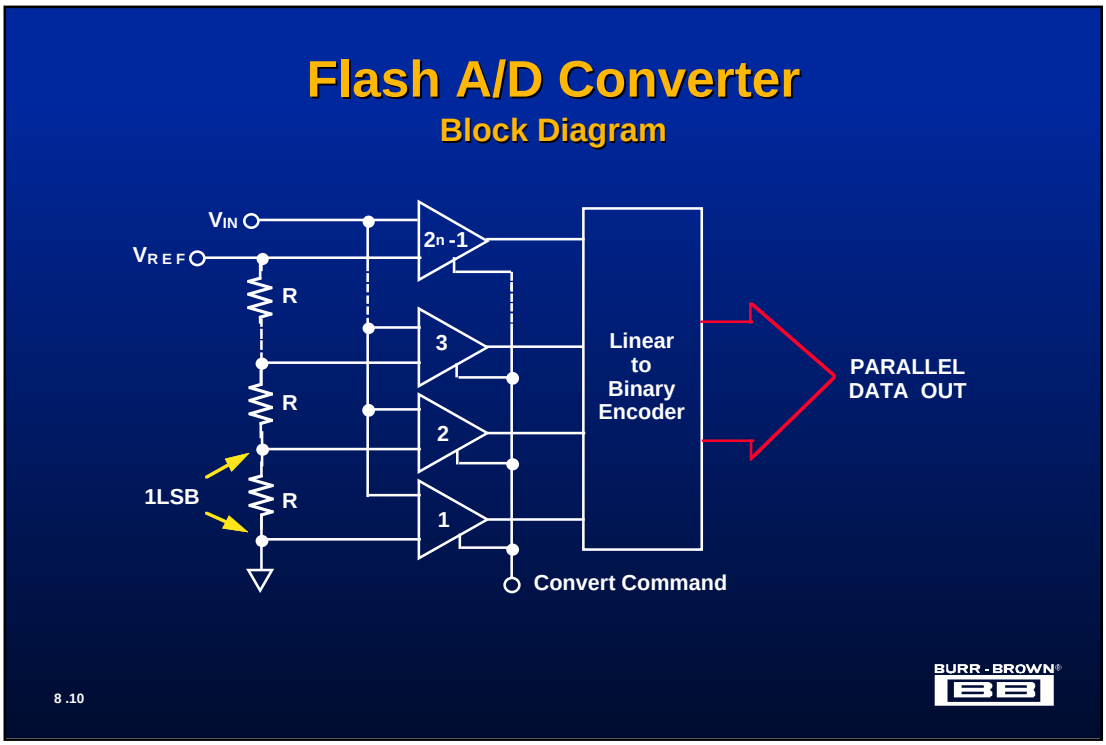


This product matrix shows the variety of analog-to-digital converters using the SAR architecture.

The ADS78XX family of A/D converters consist of 12- and 16-bit converters, offering different features like serial and parallel outputs, autocalibration, power down mode and more.

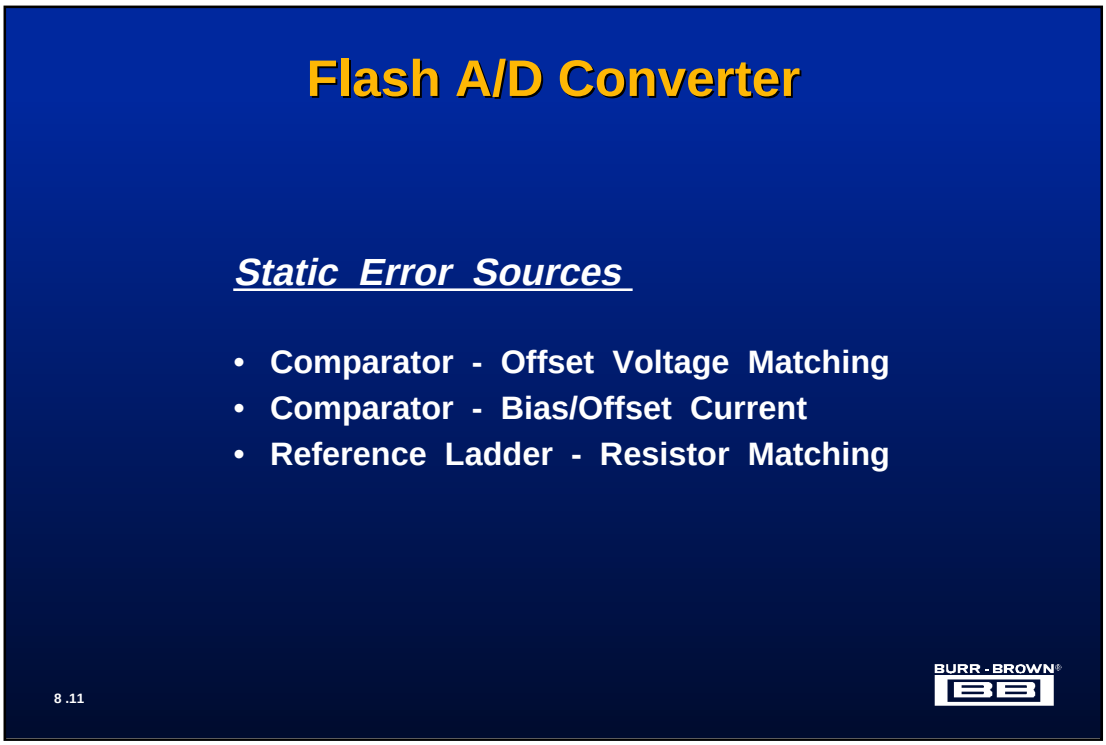
The converter with the highest resolution, PCM1750 is primarily designed for audio applications.

The lead in terms of conversion speed is held by the ADC601, a 12-bit 0.9µs converter. Its unique two-chip design utilizes a bipolar thin film IC to preserve high speed analog accuracy and a high speed CMOS IC to perform the digital logic control.



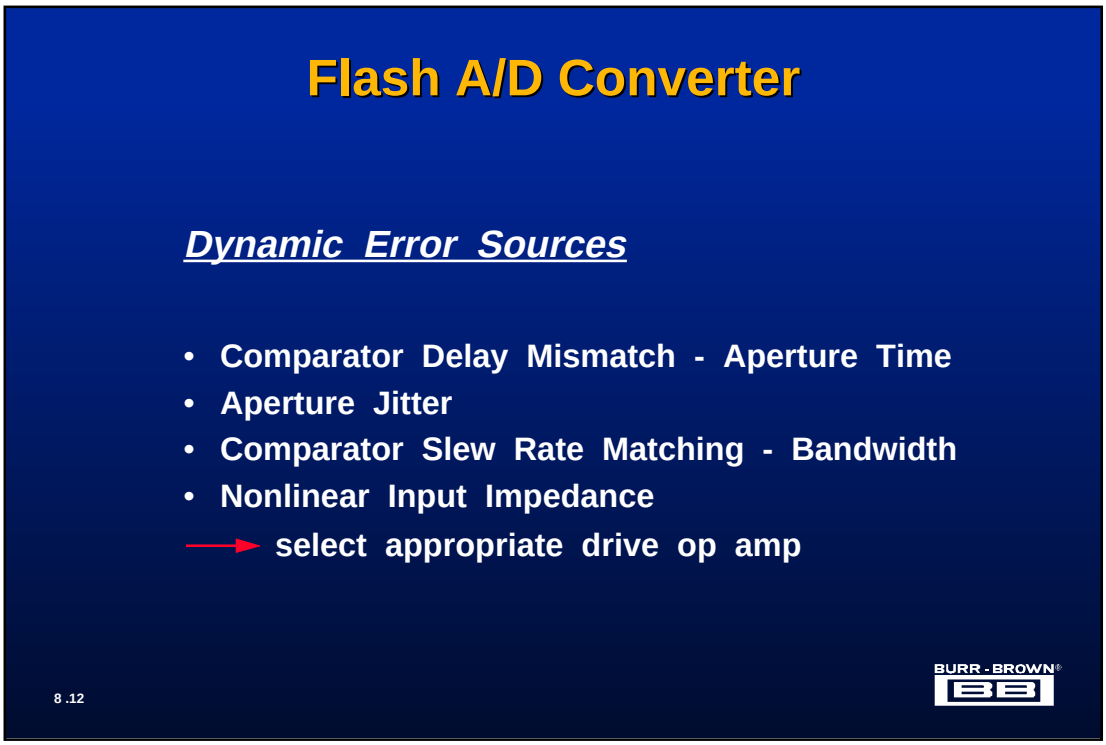
The fastest of all types of high speed analog-to-digital converters, and perhaps the easiest to understand, is the flash or parallel type of converter. The flash is considered to be the fastest A/D converter because the conversion takes place in a single cycle, hence the name “Flash”. The resolution of flash converters tend to be limited to 8-bits due to the fact that the amount of circuitry doubles every time the resolution is increased by 1-bit.

A block diagram of a flash converter is shown above. The analog input signal is applied simultaneously to the 2^n-1 latching comparators. They are arranged in a “thermometer” code fashion with each comparator’s reference biased 1LSB higher than that of the preceding comparator. The individual reference voltage is derived from a resistive voltage divider string. With the analog signal applied to the flash converter, each comparator will compare the signal level to the reference level. If the signal level is higher than the reference level the comparator will output a logic “1”. Also, the comparator will assume a logic “0” if the signal amplitude is lower than the reference. The resulting thermometer code is then converted to a conventional binary output in the subsequent logic encoder.



Even though the design of flash converters is highly repetitive in its structure, it demands a high level of matching between the parallel comparator banks. One of the major contributors to static nonlinearities is the comparator input offset voltage. The offset should be less than ±1/2LSB not to degrade the monotonicity of the converter. Similar effects could be caused by the bias and input offset currents of the comparators. Together with the resistance of the reference ladder, they will add to the offset voltage.

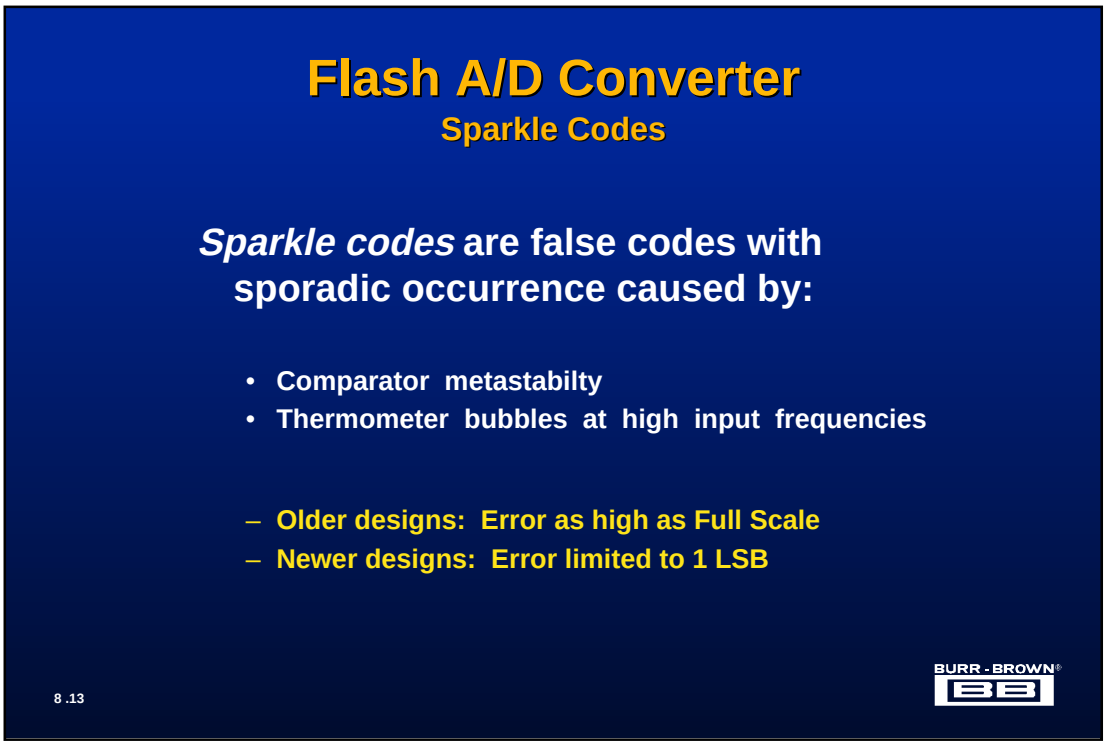
The reference voltage resistive ladder contributes as a secondary effect to the static error. The reproduction of thin film resistors is a well controlled process. Furthermore, precision laser trimming allows a relative matching of the ladder resistors in excess of the accuracy of the flash converter.



The dynamic performance is the one area that separates the flash converter from other A/D architectures. Dynamic performance is a measure of how a high speed converter is able to accurately digitize a high frequency signal. The user is required to understand how comparator delay mismatch (aperture delay distortion), aperture jitter, and input bandwidth affect the performance of the high speed converter.

Aperture time is defined as the effective point where the comparator makes its decision. Assuming an ideal flash converter is used, each comparator would latch simultaneously when the convert command is asserted. However, in an actual flash converter the delays of the logic signals are not perfectly matched. Their timing should be close enough to keep the error below one LSB.

Another source of dynamic error is the non-linear input capacitance. This input capacitance is caused by the many parallel impedances of the comparators. The problem arises because the capacitance shows a signal dependent behavior. Driving the input of a flash converter often requires a small value resistor between the driving op amp and the A/D input in order to isolate the dynamic capacitance from the op amp output.

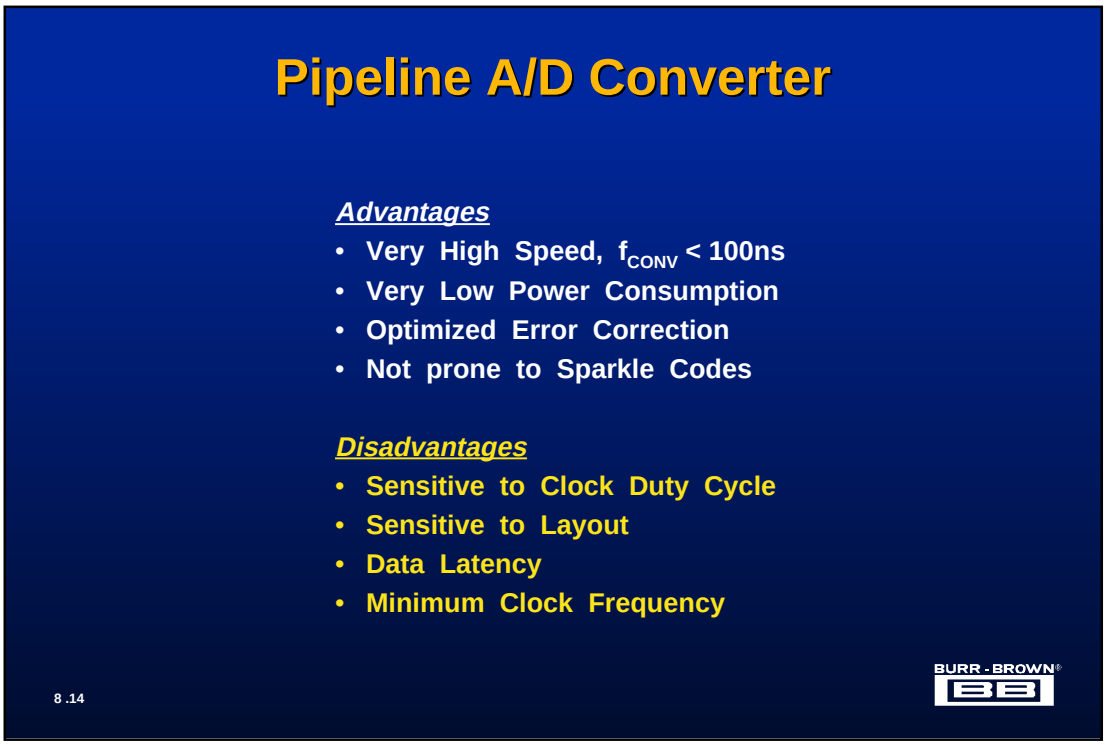


One of the main concerns in the design of digital communication systems using high speed A/D converters is the measure of the bit error rate (BER). Flash A/D converters have been known to produce false codes, which are also called “Sparkle Codes”. The expression sparkle code was originated in the imaging field where the false codes created by the flash converter caused small white dots on a TV screen. Sparkle codes are random error codes with a sporadic occurrence. Their magnitude may often approach the full scale range. Basically, there are two sources of sparkle codes within a flash converter: comparator metastable states and thermometer code bubbles.

A metastability of the comparator occurs if the comparator output falls between the logic 1 and logic 0 threshold of the digital encoding logic. Here, the magnitude of the error code depends on the location of the comparator in the comparator bank. If it is the comparator for the MSB the error will reach the full scale.

Another source of sparkle codes are the so called thermometer bubbles. Under normal operation, all of the comparators in the flash converter will produce a specific sequence of ones up to a certain point in the input range, and will produce a sequence of zeros once exceeding this point. In the encoder the thermometer code is translated into a binary word. At higher input frequencies delay mismatches between the comparators may produce sporadic false codes by changing ones into zeros and vice versa. Because the encoder is not able to detect those error codes it will result in a bubble, which is an out of sequence code. At the output of the converter it will also appear as a sparkle code.

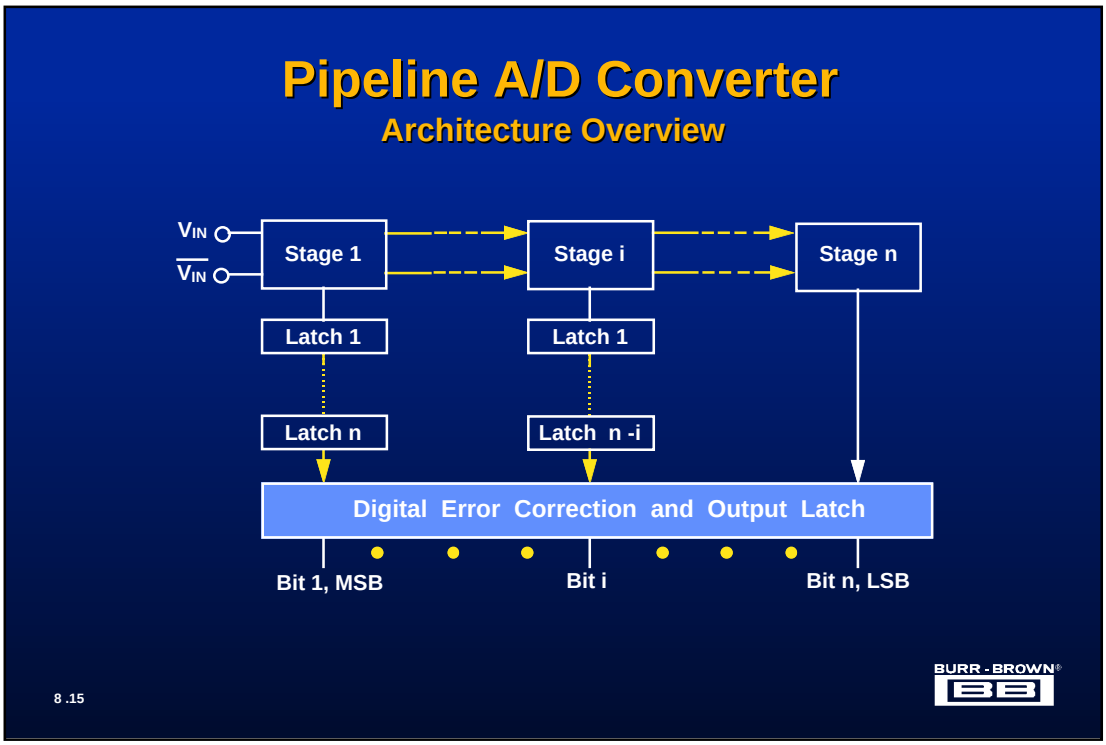
Both instances depend on the design of the flash converter, and techniques have been developed to keep the magnitude of sparkle codes to only one LSB.



The last architecture that will be discussed is the pipeline technique, which can be considered also another derivative of the “one bit” comparator topology of the successive approximation converter and the “all bits at once” design of the flash ADC. As the next logical step after the sub-ranging architecture, pipeline converters are just beginning to emerge on a broad basis throughout the IC industry, although, the proof of concept was done about eight years ago.

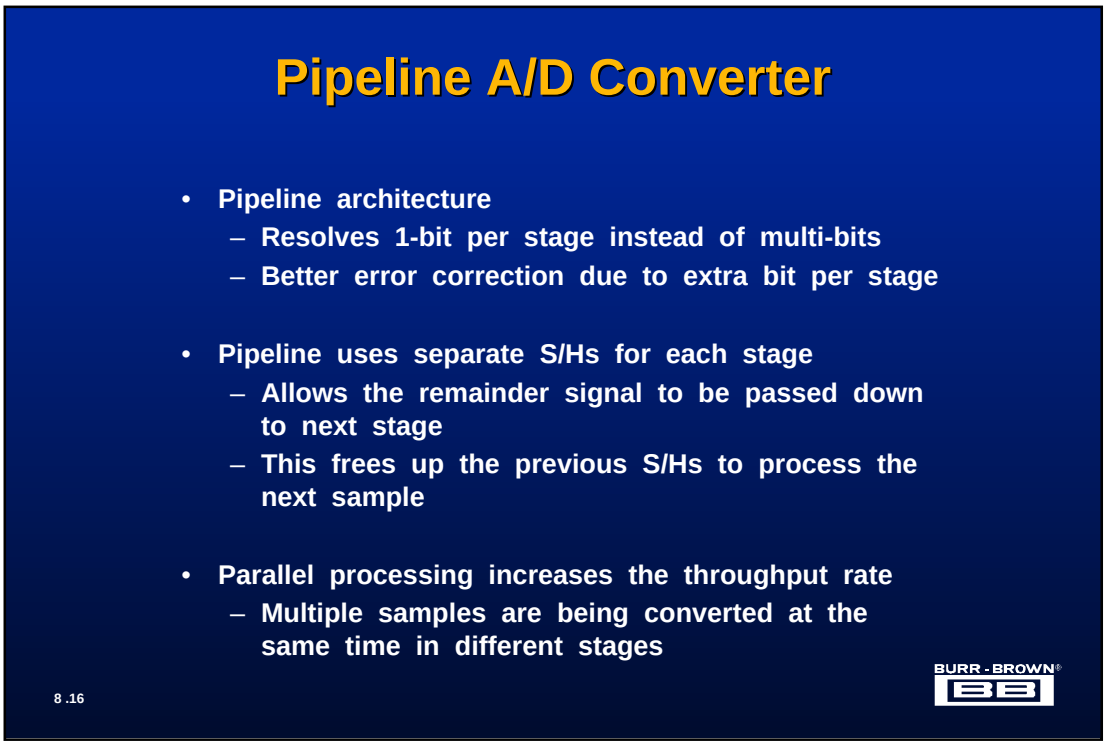
Because of their concurrent digitizing technique pipeline converters achieve comparably high conversion rates in excess of 50MHz. Built as monolithic ICs on CMOS processes one of their biggest advantage is the low power consumption. This opens up the complete market of battery powered equipment.

Even though pipeline converters use the flash architecture as a subcircuit in their processing path they do not exhibit the problem with sparkle codes. This is essentially due to the fact that each flash converter is of low resolution (1 to 2 bits). This means that the number of comparators is very small, which results in a good separation of their threshold voltages compared to pure flash converter. The appearance of false codes, or “sparkle codes” due to the false trigger of one of the comparators is not an issue with pipeline A/D converter.

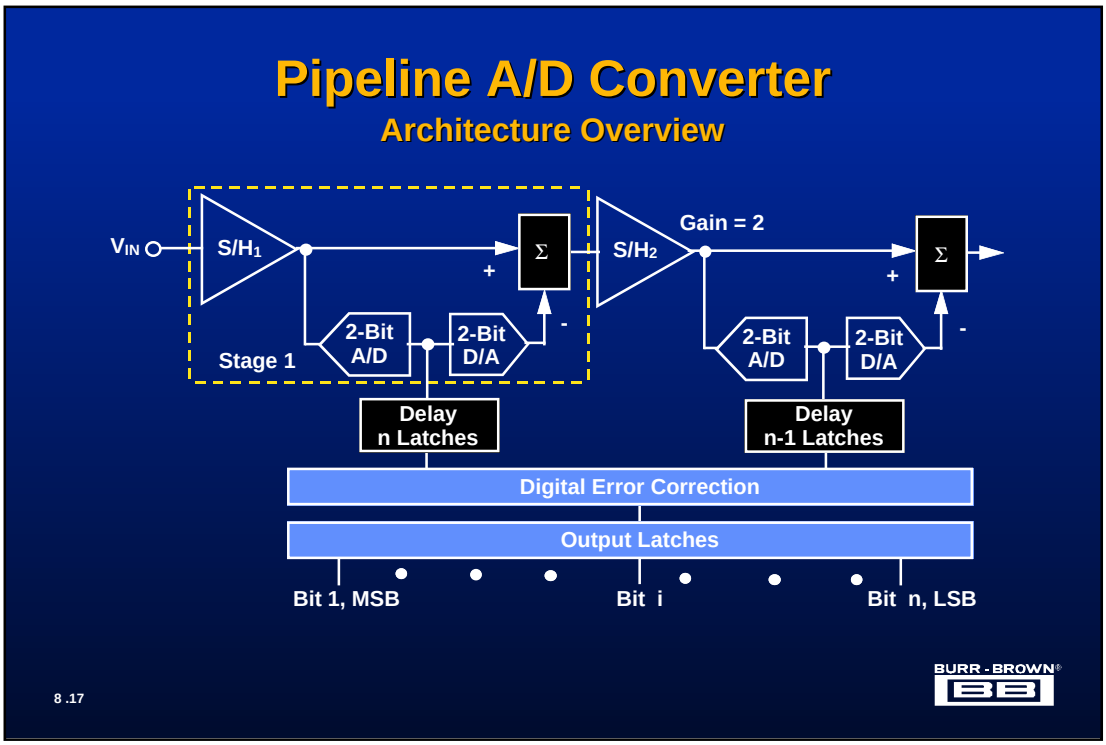


A pipeline A/D converter consists of a number of consecutive stages. The number of stages is often similar to the number of bits of resolution. The stages are similar in their function, as will be discussed later, and each stage only resolves one or two bits. Each individual stage consists of a sample and hold, a low resolution flash A/D converter, a low resolution D/A converter and a summing stage including an interstage amplifier for providing gain. The outputs of each stage are combined in the output latch.

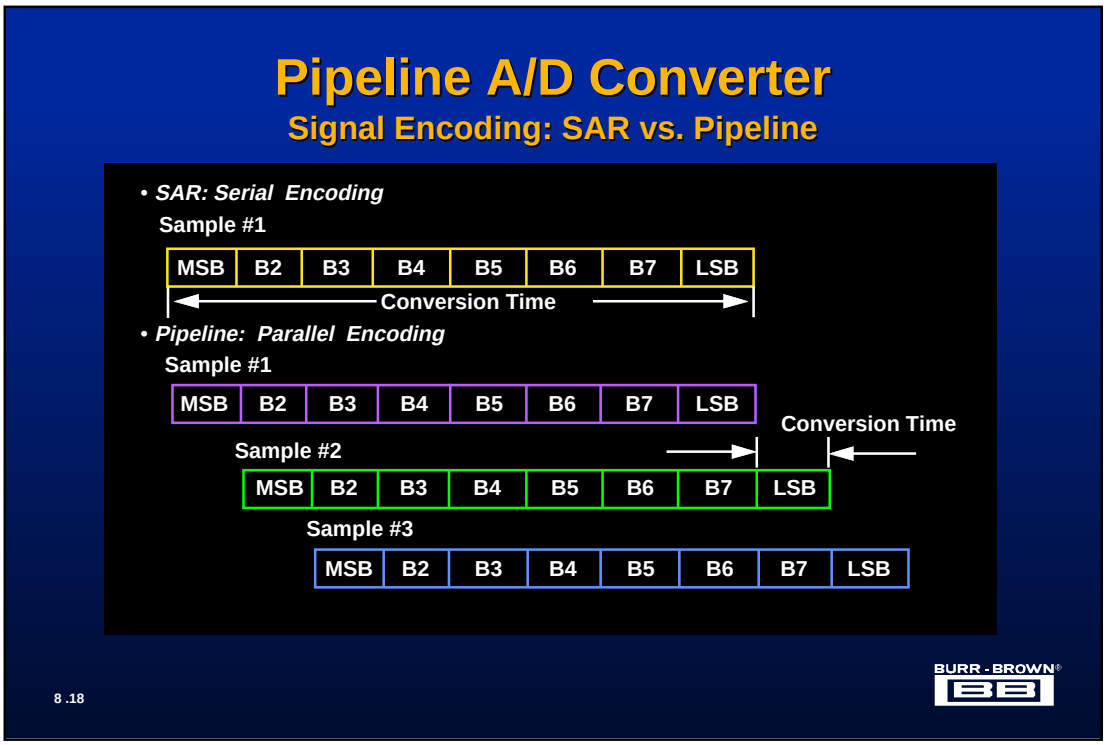
Stage 1 takes a sample of the input voltage and makes the first coarse conversion. The result is then the MSB and its digital value is fed to the first latch (Latch 1). As the residue of the first stage gets resolved in the subsequent n-stages the MSB value is rippled through the n number of latches in order to coincide with the end of the conversion of the last stage. Then all data bits are latched in the output and are available to the data bus.



Due to the small dimensions (die size) and low power consumption, the pipeline architecture is more suitable for high-resolution applications than flash converters, but is also susceptible to circuit imperfections, such as offset/gain error, and nonlinearities.

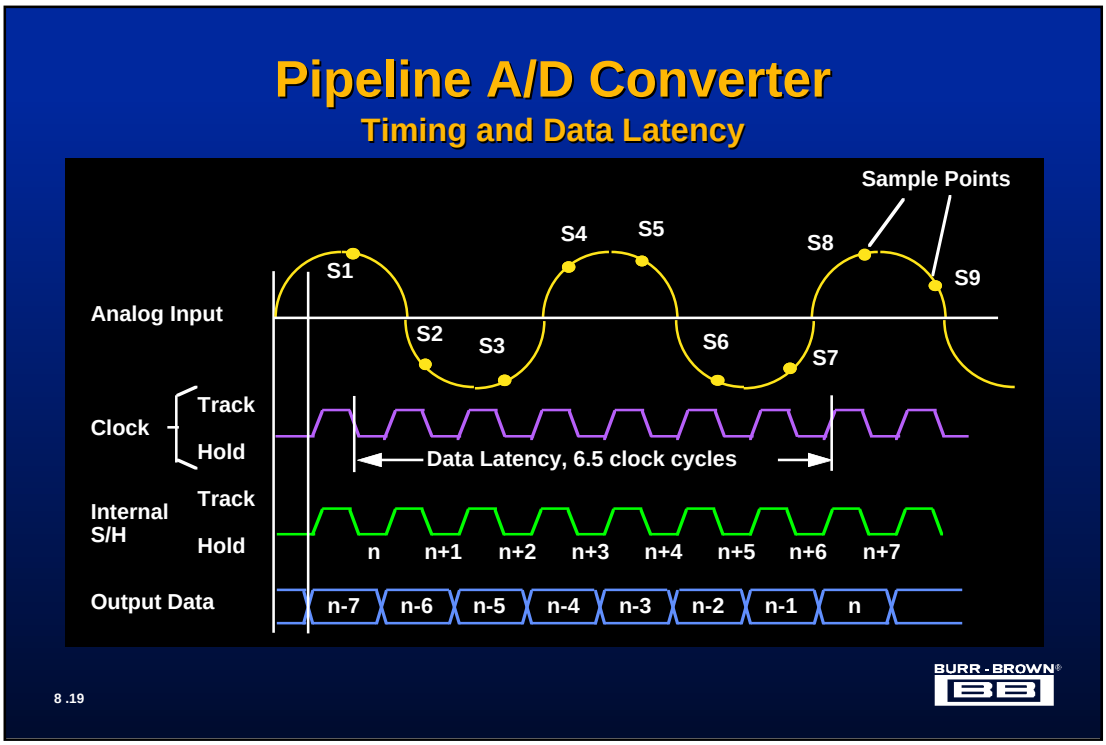


This figure depicts the conceptual blocks inside a pipeline A/D converter. The structure is highly repetitive where each of the pipeline stages consists of a S/H, a flash A/D converter, a D/A converter, a subtractor including a gain stage and latches for delay. Both, the A/D and D/A converter are of low resolution, in this case 2 bits. To begin a conversion, the input is sampled and held. The held input is then converted into a digital code by the first stage low resolution A/D converter and back into an analog signal by the D/A converter. The difference between the D/A output and the held input is the residue that is amplified and sent to the next stage where this process is repeated. At any instant, while the first stage processes the current input sample, the second stage processes the amplified residue of the previous input sample from the first stage. Because sequential stages simultaneously work on residues from successively sampled inputs, the digital outputs from each stage correspond to input samples at different times. Digital latches are needed to synchronize the outputs from the n-stages.



The main advantage of pipeline ADCs is that they can provide a high throughput rate with moderate IC design complexity and low power consumption. This is because of the concurrent operation of the n-stages. The associated “data latency” is not a limitation in most applications. Two main clock phases are required per conversion; because the pipeline ADC uses flash converters. Therefore the maximum throughput rate can be high.

After the initial data latency time, the data representing each succeeding sample is output with every following clock pulse.



To obtain the best performance from pipelined A/D converter the designer needs to make careful considerations about the timing and the clock source. This is basically true for all high speed A/D converter architectures. Clock jitter can introduce a significant error and needs to be kept low to avoid a degradation of the resolution.

With pipeline A/D converter the rising and the falling clock edge are used to initiate certain operations. Each converter stage in the pipeline will be sampling during one phase and amplifying in the other phase. The internal S/H clock applied to each sub-converter is offset by 180° phase from the previous stage clock signal with the result that alternate stages will perform the same operation (concurrent operation).

The duty cycle of the external clock should be held at 50% with a low jitter of less than 3.5ps (for the 40MHz ADS8XX) especially when digitizing a high frequency input signal and operating the maximum sample rate. A deviation from the 50% duty cycle will effectively shorten some of the interstage allowed settling times, thus degrading the SNR and DNL performance.

The first valid digital data of the pipeline architecture will have an associated delay before it becomes available at the bus. This delay is called “Data Latency” and is dependent on the number of internal converter stages . For example, the ADS8XX has a data latency of 6.5 clocks.

Pipeline A/D Converter

The ADS8XX Converter Family

	Resolution	F_{CONV}	SNR @ 0.5MHz	Power
ADS800	12-Bit	40MHz	64dB	0.39W
ADS801	12-Bit	25MHz	66dB	0.27W
ADS802	12-Bit	10MHz	67dB	0.25W
ADS820	10-Bit	20MHz	59dB	0.19W
ADS821	10-Bit	40MHz	61dB	0.38W

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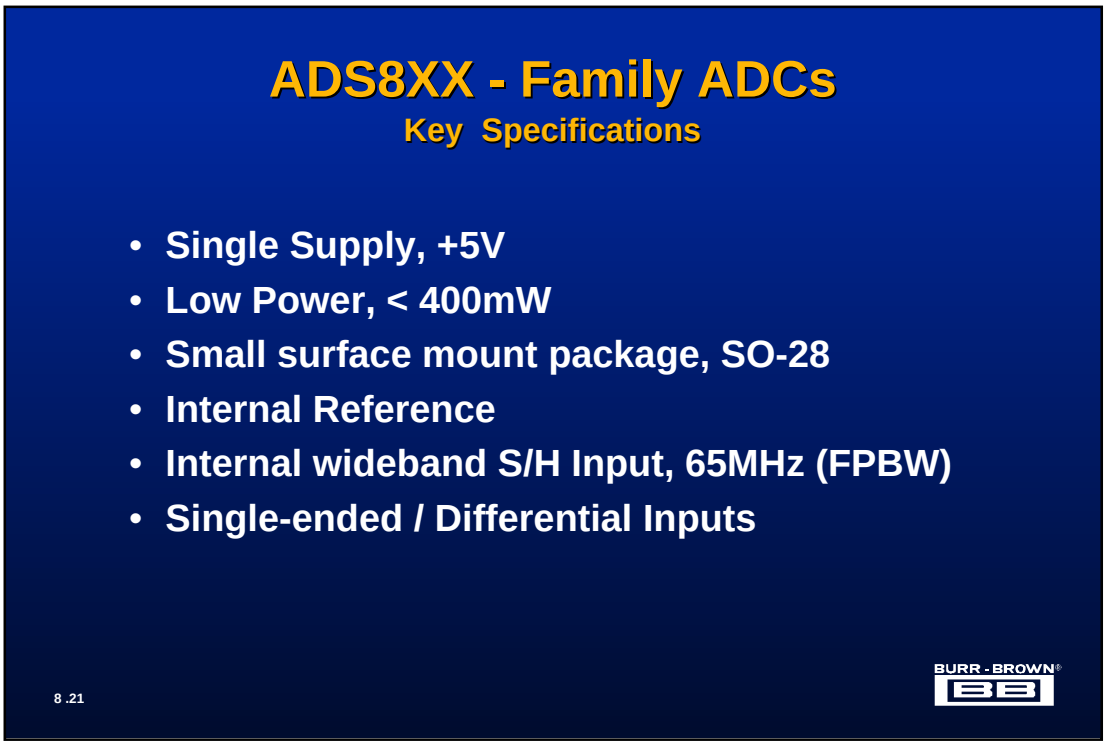
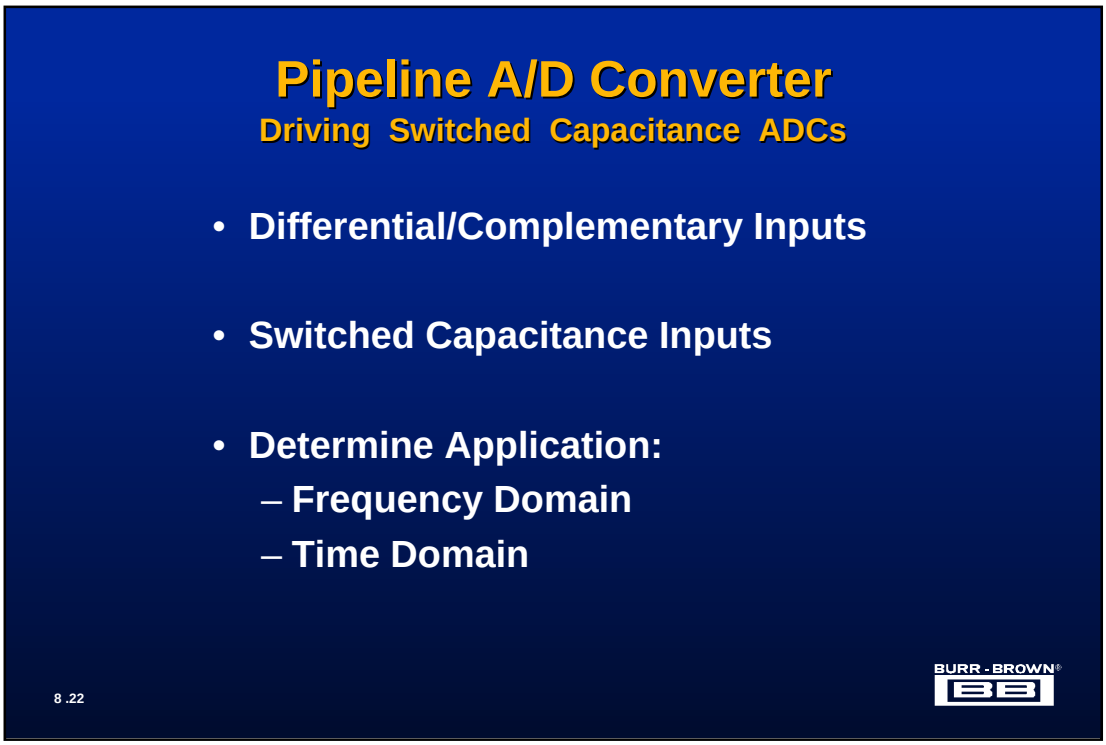
The new ADS8XX Family of high speed A/D converter features the previously described pipeline architecture. This makes it possible for the ADS8XX to achieve 12-bits of resolution with a conversion rate of 40Msps while only consuming about 390mW. As a performance measure the spurious-free dynamic range is listed for the five models as well. The following pages will discuss the ADS8XX family in more detail.



All of the five models within the ADS8XX family are monolithic ICs built with a small geometry (0.6µm) CMOS process. This allows those converters to operate on a +5V single supply voltages with a very low power consumption. This parameter varies from part to part, as shown on the previous page, and influences the dynamic performance to some extend. The ADS8XX converter come complete with an internal reference, a 10- or 12-bit quantizer, a wideband sample and hold amplifier and 3-state outputs.



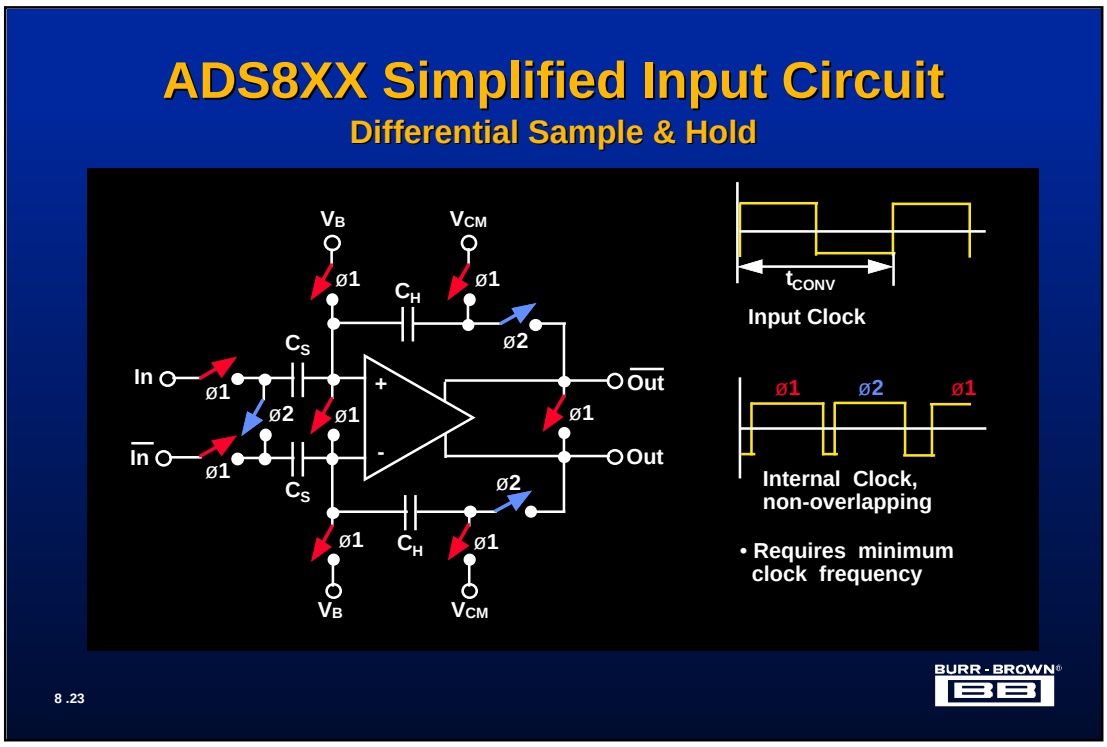
Even though the new pipeline technique significantly simplifies the power supply management, it imposes another set of problems. One of the main differences to the previously discussed architectures is the differential input structure; one non-inverting input and one complementary input. Also, a common observation at the switched inputs of those ADCs is that they generate small current spikes during sampling. This issue will be discussed later in detail.

Some applications will require low distortion and spurs (frequency domain), others need low noise with excellent time domain behavior. These performance specifications should be considered as a first step during the design phase in order to optimize the input driver. Here some examples:

• Communication systems - They typically involve spectral analysis. This requires that the entire signal chain is optimized in terms of the harmonic distortion (THD) and spurious-free dynamic range (SFDR). The signal content is usually confined to half the sampling rate (<= Nyquist frequency).

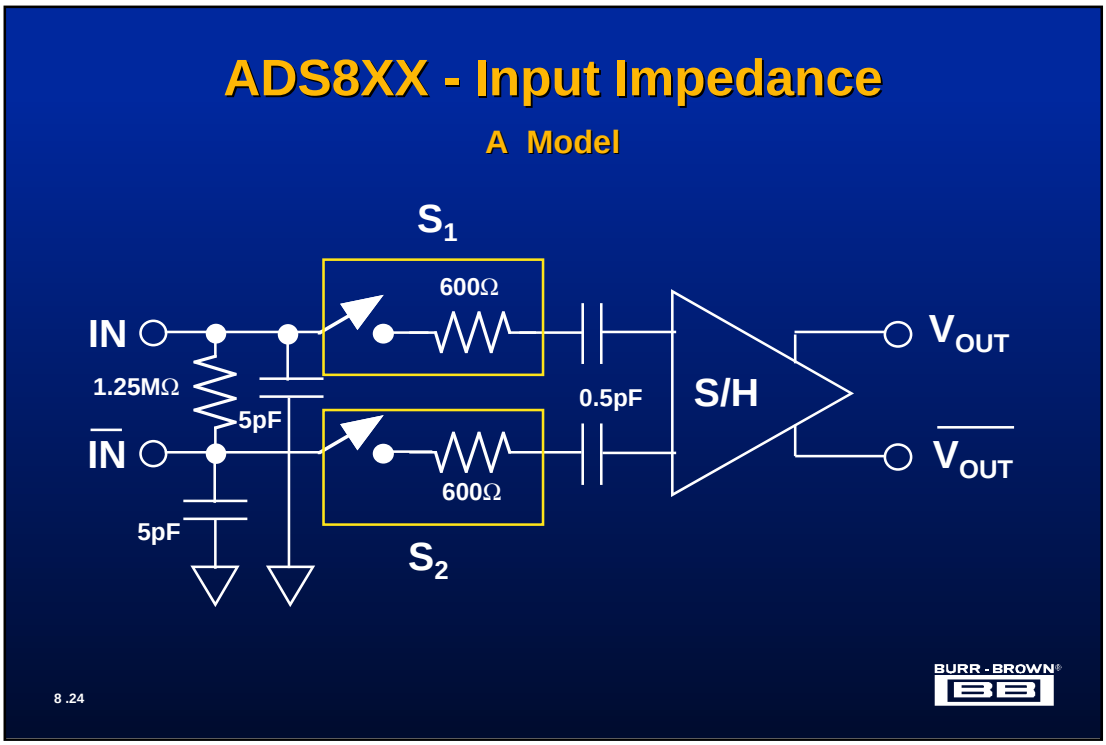
• CCD-based imaging - A typical example of a time domain application. Here the requirements focus on specifications like noise, wide bandwidth and fast transient response to ensure fast settling. Specifications like THD, SFDR and SNR may be sacrificed.

• Data acquisition systems (DSO) - A standard application where both the time and frequency domain specifications are important, e.g. low spurs and wide dynamic range. Not only is the contribution of the voltage and current noise of concern, but also the phase noise, such as that generated from aperture jitter.



In order to understand the performance requirements of the external input driver circuit, a look inside the ADS8XX will be helpful. Shown here is the simplified input circuit, the differential switched capacitance sample and hold. The switches are controlled by an internal clock which is a non-overlapping two phase signal, ø1 and ø2, derived from the master clock. During the sampling phase, ø1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are charged to the common-mode voltage, V_{CM}. At the falling edge of ø1 the input signal is sampled on the input plates of the sampling capacitors. In the next clock phase, ø2, the two input plates are connected together and the holding capacitors are switched to the op amp output nodes. The charge then redistributes between C_S and C_H completing one sample and hold cycle. The output is a fully differential DC representation of the analog input. The circuit not only performs the sample and hold function but will also convert a single ended input to a fully differential output for the converter core.

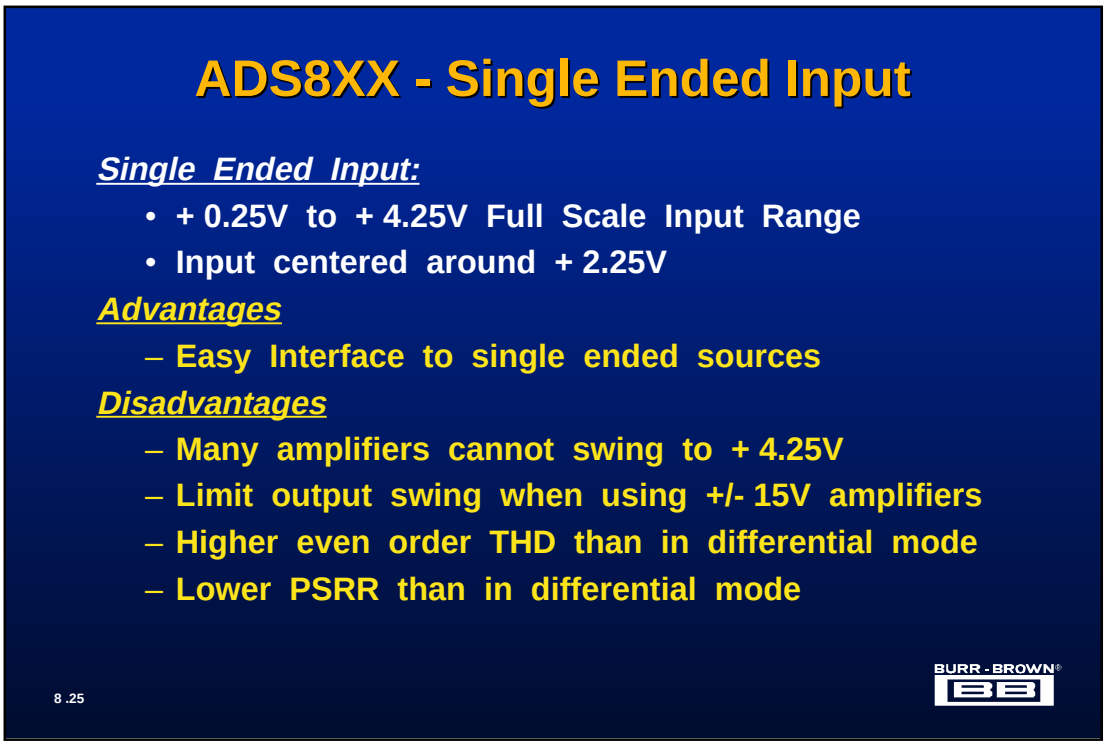
Pipeline ADCs with their switched capacitance structure suffer from one limitation: they usually have a lower limit of their clock frequency. At very low frequencies or when pausing the clock (burst mode), leakage currents will affect the charge redistribution in the capacitors up to the point where the signal becomes invalid. In the worst case the internal sample and holds can droop to the rails with no clock. Therefore, without appropriate “charge refresh” the dynamic performance will degrade. Burst mode operations are possible, but the user should keep in mind that he eventually has to flush the pipeline each time the clock was stopped. This is required in order to clear out invalid data as a consequence of the data latency period.



This slide depicts the input impedance of the switched capacitance input circuit common to all the discussed pipelined converter. Using a simple model two possible situations can be evaluated: the first one when the converter is in normal operation with a continuous running clock. And secondly, when the converter is inactive e.g. with a paused clock.

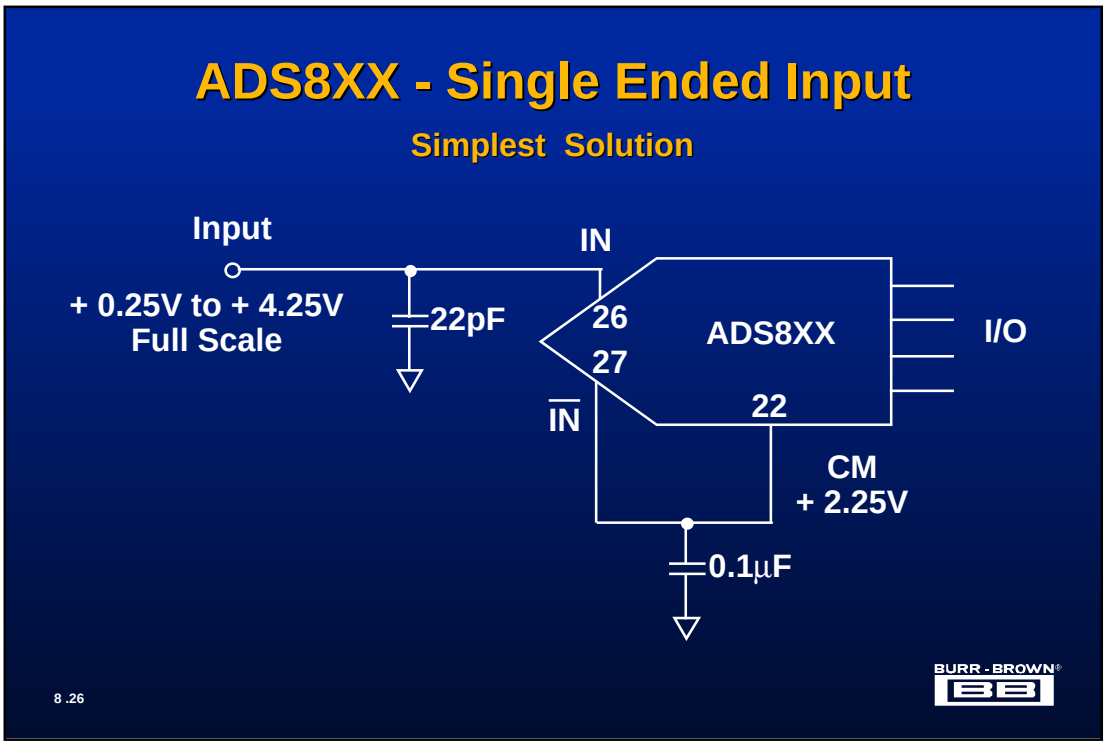
In the first case the two switches, S_1 and S_2, will exhibit an On-resistance, R_{ON}, of about 600Ω, which varies slightly over the input voltage range. Together with the input capacitance, which includes parasitic capacitance, an RC time constant is created. This also accounts for a high frequency roll off in the transfer function of the input of the ADC. For example, the ADS8XX show a small signal bandwidth of 400MHz. The main limitation of the achievable input bandwidth is usually the moderate slew rate of the internal CMOS op amps, in this case about 500V/µs.

If no clock signal is applied the switches are open. Now the input impedance seen by the external driver is modeled by a 1.25MΩ resistor and a 5pF capacitor to ground on each of the inputs.



At the first glance, using the ADS8XX with a single ended input seems to be the most attractive configuration, because it would require only a minimum of external components. However, in this configuration the driving circuit would be required to deliver double the full scale swing as would be needed for differential inputs - a swing from +0.25V to +4.25V. This is a 4V peak-to-peak swing compared to a +1.25V to +3.25V range in the differential mode where there are two inputs of opposite phase (180°).

All A/D converter within the ADS8XX family operate on a single +5V supply. Op amps, that work of dual 12V or 15V supplies ensures that the input swing is limited to the maximum input range the ADC rather than the drawing amplifier. With this configuration, the users must ensure that the maximum input range of the ADC is not violated. The maximum input range for the ADS8XX is ($+V_S$ - 0.3V) and 0V. The inputs of the ADS8XX family converter are protected against overvoltage and ESD by internal ESD diodes. If the voltage at the inputs exceed the maximum ratings the diodes will conduct.



This configuration of the ADS8XX shows the simplest application of the converter. Configured for single ended input operation the input sample and hold performs the function of converting the single ended input signal into the differential signal needed by the subsequent internal ADC stages. The common-mode voltage of +2.25V available at pin 22 (MIDREF) is directly fed into the complementary input, pin 27 ($\overline{IN}$). Using this as the level shifted bipolar zero the input signal swings between +0.25V and +4.25V.

The input full scale range may be reduced. This can be achieved by forcing the “positive full scale reference” and the “negative full scale reference” to different voltages, other than +1.25V and +3.25V.

ADS8XX - Differential Input

Differential Input:

- + 1.25V to + 3.25V Full Scale Input Range
- Each Input centered around + 2.25V

Advantages:

- Easier for + 5V amplifiers to swing to Full Scale
- Low 2nd Harmonic Distortion due to even order cancellation
- Better PSRR than single-ended

Disadvantages:

- Usually requires external circuitry for single ended to differential conversion

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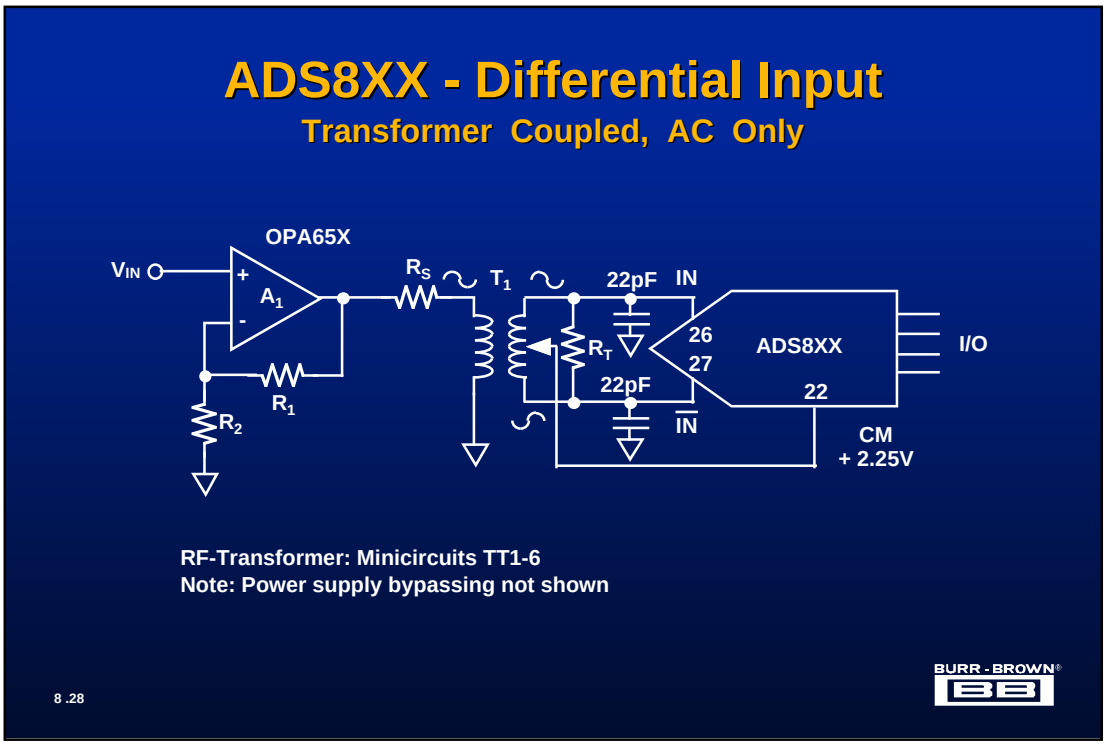
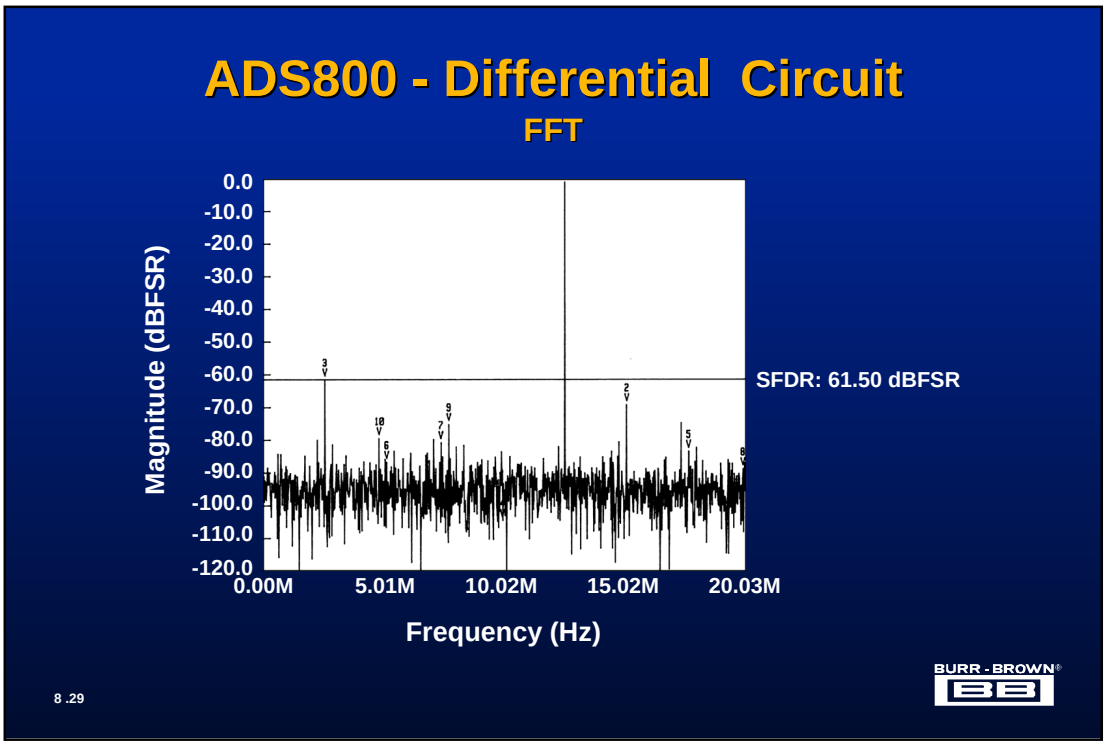
Having a differential input A/D requires an understanding of the advantages and disadvantages associated with the topology. To achieve the best dynamic performance it is recommended that the differential inputs be used. For example, the harmonic distortion and the power supply rejection is improved compared to the single ended operation. This is because of the cancellation effect all circuits with a differential input structure have to error signals that appear in the signal path and are of equal appearance (frequency and magnitude).

One requirement for the differential interface circuit is that it creates two signals which are equal in amplitude but 180° out of phase. This in fact is an advantage because it reduces the output voltage swing for each of the driver op amps in half. Now, they only have to provide a 2Vp-p swing compared to the 4Vp-p swing needed when driving the ADS8XX single ended.

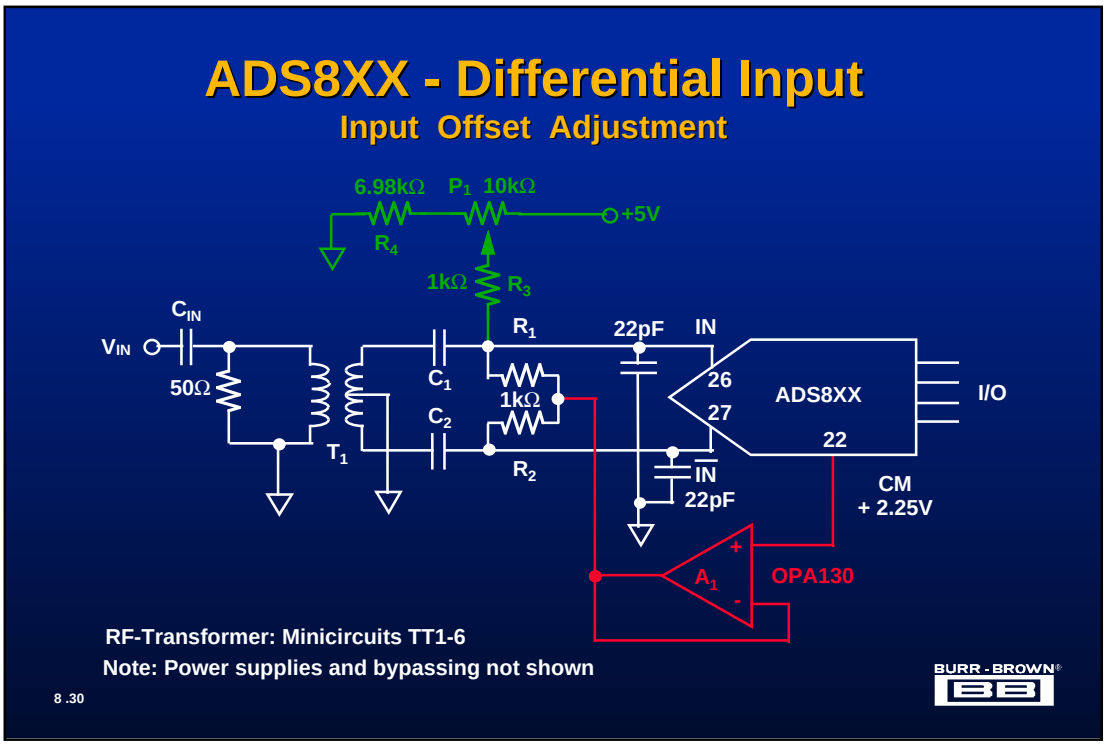


As already mentioned, all the ADS8XX converters have differential inputs centered around an offsetted common-mode voltage, “CM”. CM is the mid-scale reference voltage of +2.25V. For those applications where the input driver and the ADC do not need to be DC coupled, a RF transformer is the easiest way to implement the single ended to differential conversion. A transformer with a center tap on the secondary side, like the TT1-6 from Mini-Circuits, provides a very convenient way to apply the common-mode voltage to the inputs of the ADS8XX.

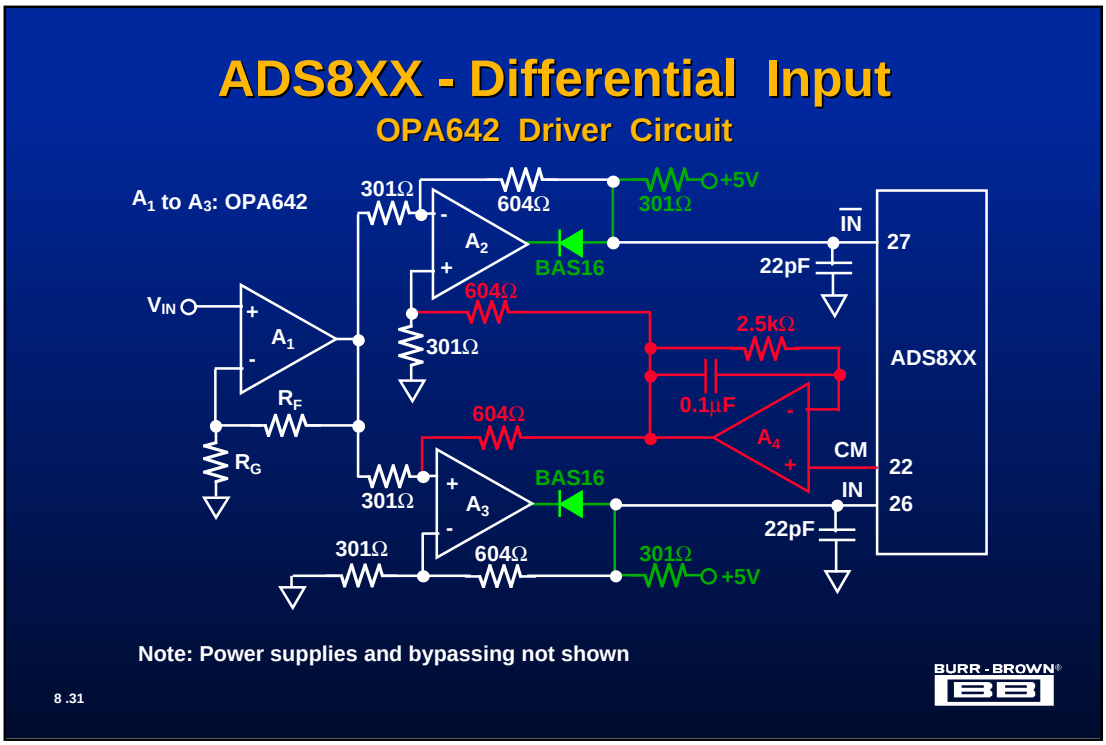


The FFT response of the ADS800 with a differential input using a transformer to couple the signal to the input of the A/D converter is shown above. In this test the input frequency was 12.5MHz with a sampling frequency of 40.1MHz. The number of data points in the test equals 2048 samples. In this test the following results were measured:

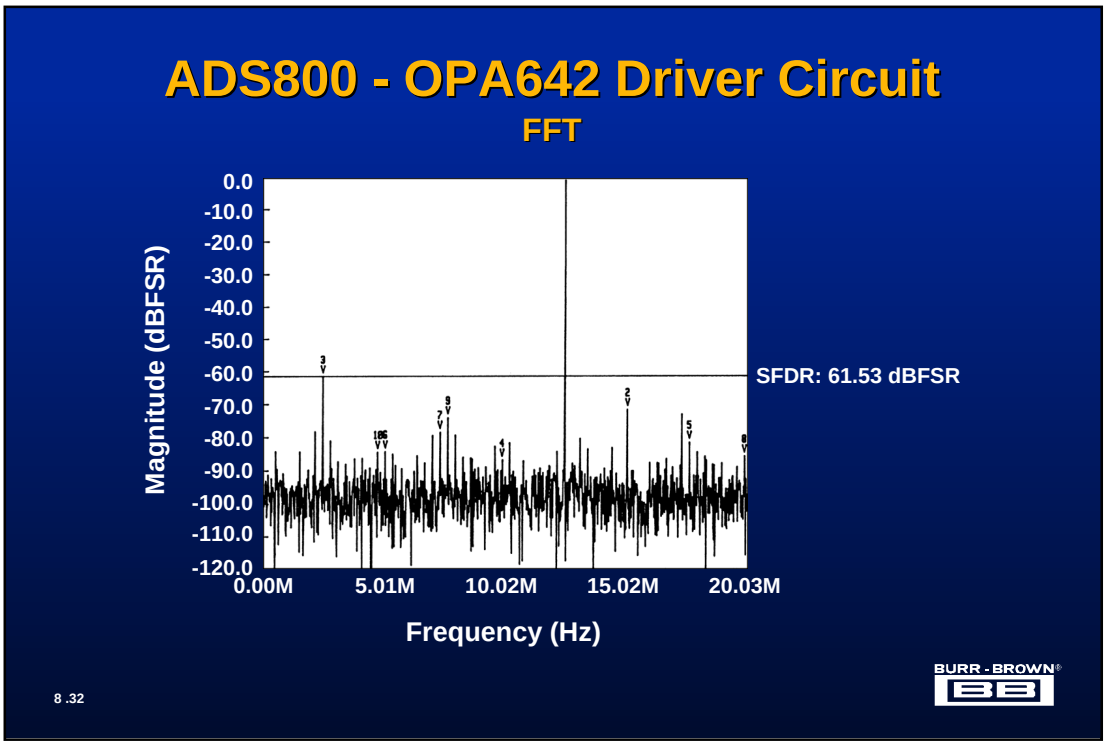
Fundamental =	**-0.99 dBFSR**
2nd Harmonic =	**-69.22 dBFSR**
3rd Harmonic =	**-61.50 dBFSR**
4th Harmonic =	**-104.54 dBFSR**
5th Harmonic =	**-83.43 dBFSR**
6th Harmonic =	**-86.69 dBFSR**
SFDR =	**61.50 dBFSR**
THD(9) =	**-59.53 dBc**
SNR =	**61.32 dB**
SINAD =	**57.32 dB**



Some applications may require an adjustment capability of the ADSs input offset voltage, which typically is 1% of the full scale range, or +/-40mV. Based on the transformer coupled input configuration a circuit with offset adjustment is shown here. The two capacitors, C_1 and C_2, are needed to block the DC path through the transformer to ground. This is necessary, because the offset can only be adjusted by changing the voltage level of one of the inputs relative to the other. Without the capacitors the voltage level on both inputs would change simultaneously, which has no effect to the offset of the ADC. Buffered by amplifier A_1 the common-mode voltage of +2.25V is applied to input $\overline{IN}$. Because the DC input impedance of this input is high no current flows through resistor R_2, hence the full +2.25V will also be at $\overline{IN}$. For the other input, IN, the DC level will be different than +2.25V depending on the position of the trim potentiometer P_1. Here, a current flows through resistor R_1 and R_3 to the low output impedance of the op amp A_1. Because of the fact that the CM pin has an impedance of about 2kΩ, it is necessary to have the buffer op amp. With the shown resistor values, the nominal trim range will be approximately + 2.25V±0.25V.

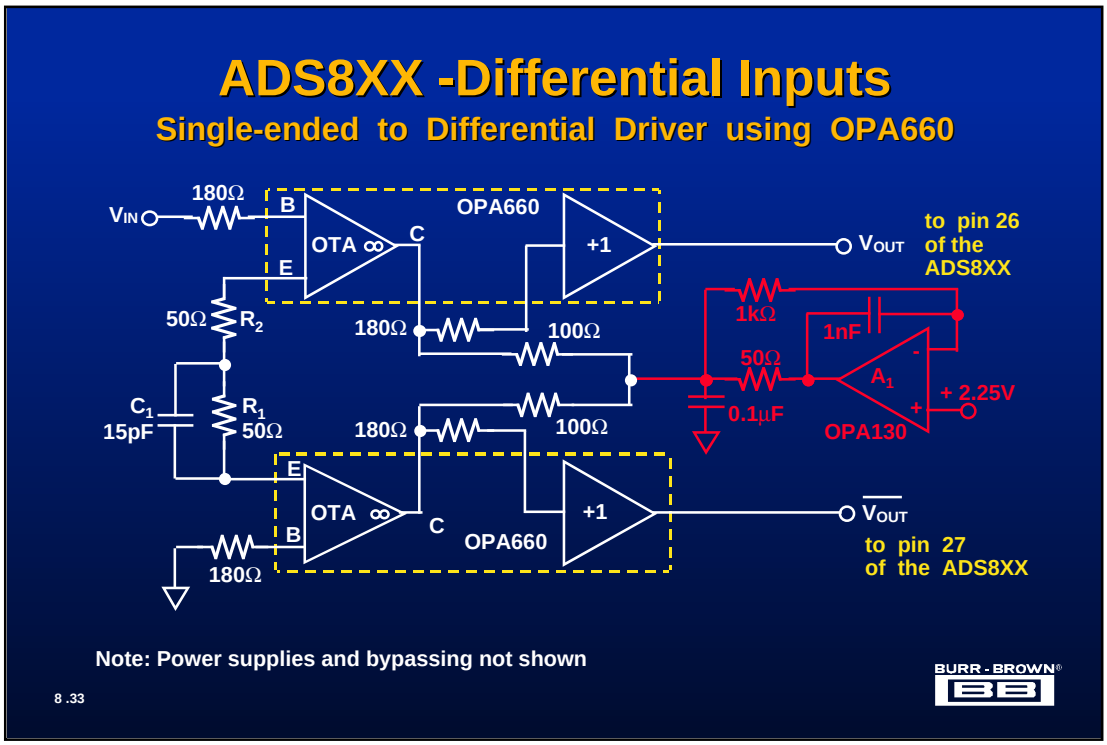


If the signal needs to be DC coupled to the input of the ADS8XX, an operational amplifier interface circuit is required. In the differential input mode, any single-ended signal needs to be converted into a differential signal. This can be accomplished by using two op amps, one (A_3) in the non-inverting mode for the non-inverting input (IN) and the other amplifier, A_2, in inverting mode for the complementary input ($\overline{IN}$). The low distortion circuit shown here will provide the necessary input shifting required for signals centered around ground, as well as a diode for output level shifting to guarantee a low distortion +3.25V output swing. Another amplifier, like the OPA650, might be used in place of the OPA642 if lowest distortion is not of prime concern. If level shifting circuits are not required, care must be taken to select operational amplifiers that have the required performance when swinging to +3.25V with a ±5V supply.

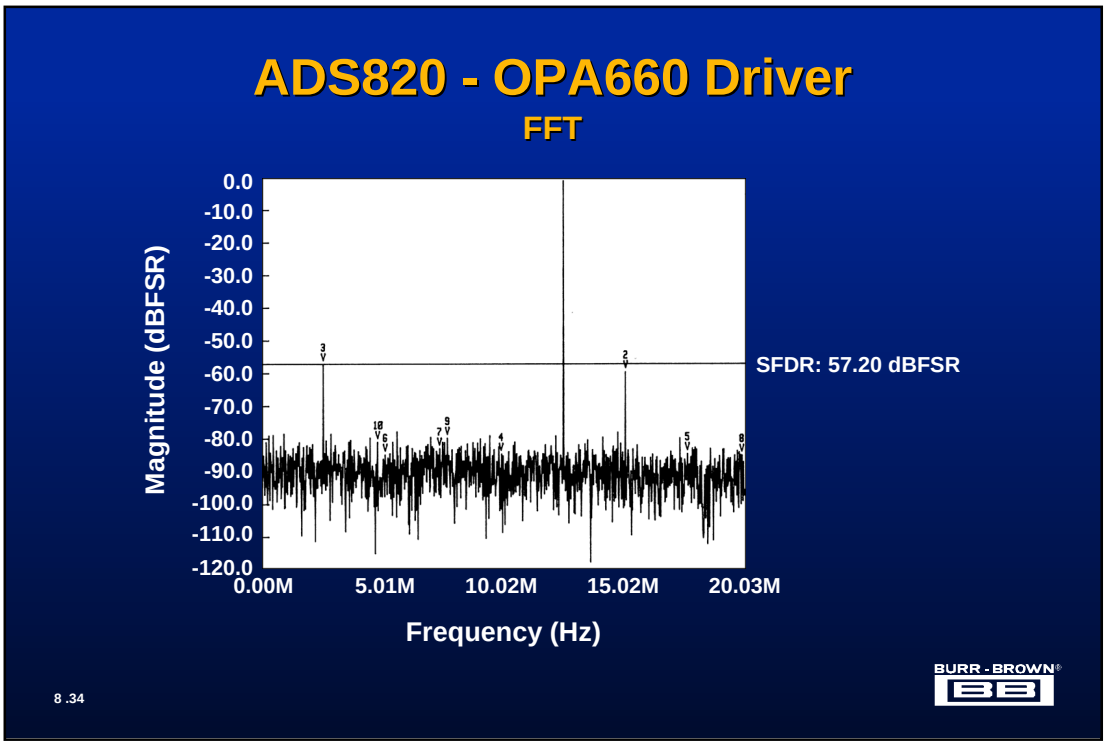


The FFT response of the ADS800 with the driver circuit shown in the previous slide is shown above. In this test the input frequency is again 12.5MHz with a sampling frequency of 40.1MHz. The number of data points in the test equals 2048 samples. This configuration gives comparable results as the test with a single-ended input circuit using the transformer. In this test the following results were measured:

Fundamental =	**-1.06 dBFSR**
2nd Harmonic =	**-71.70 dBFSR**
3rd Harmonic =	**-61.53 dBFSR**
4th Harmonic =	**-86.87 dBFSR**
5th Harmonic =	**-81.56 dBFSR**
6th Harmonic =	**-84.29 dBFSR**
SFDR =	**61.53 dBFSR**
THD(9) =	**-59.68 dBc**
SNR =	**62.79 dB**
SINAD =	**57.95 dB**

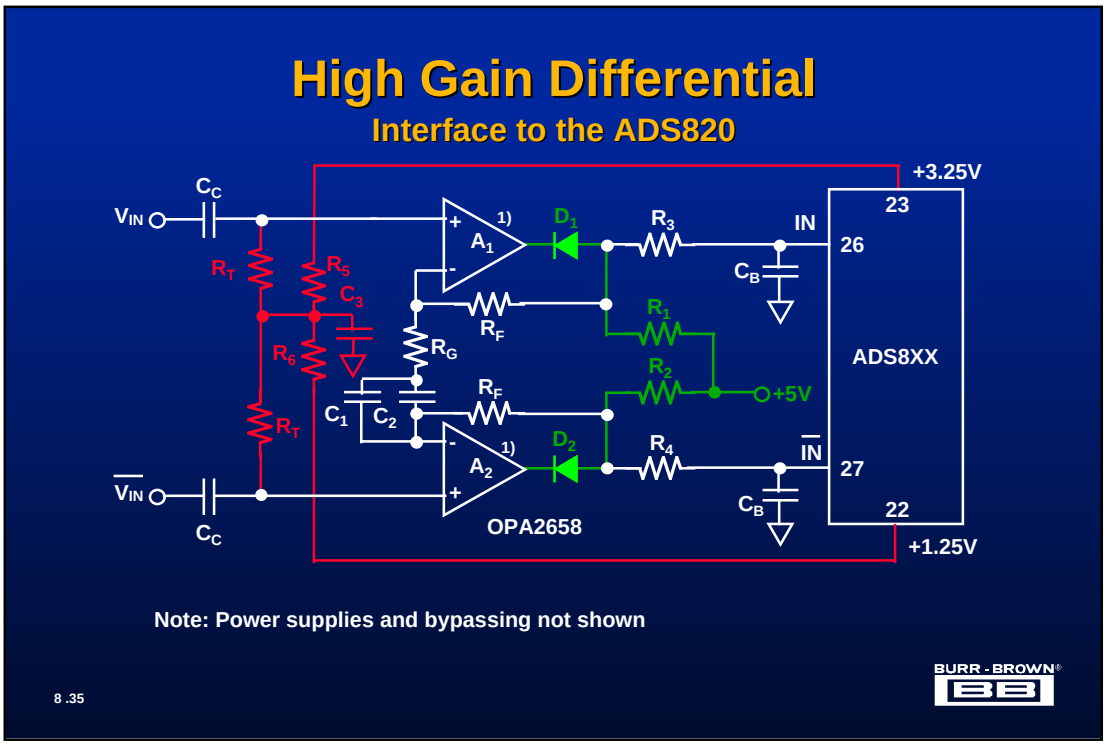


Using current sources avoids the problem of the limited output swing of class AB output stage amplifiers. The OPA660 is a wideband operational transconductance amplifier and consists of two circuit blocks: the OTA and the buffer (+1). The OTA section is a voltage controlled current source and the output compliance voltage is typically ±4.7V on a ±5V supply. The shown circuit uses two OPA660 to convert the single ended input into a differential output signal. The internal buffer are used to buffer the collector output terminals and to obtain a voltage rather than a current to drive the ADS8XX. The buffer output still offers a swing ±4V into the A/D converter. Amplifier A_1 adds the necessary common-mode voltage of +2.25V, after doing filtering, to the signal at each of the buffer inputs. The gain of the OPA660s is set by R_1, R_2 and C_1 according to the equation: $V_{OUT} = V_{IN} \bullet 100\Omega / (R_1 + R_2)$. The capacitor C_1 is optional to provide some frequency dependent gain. The gain equation is only an approximation because it does not take the internal emitter resistance into account, which is varies with the user selectable quiescent current (see the data sheet for details).



The FFT response of the ADS820 with a single-ended input using an OPA660 to couple the signal to the input of the A/D converter is shown above. As previously, this test was performed using an input frequency of 12.5MHz with a sampling frequency of 40MHz. The number of data points in the test equals 2048 samples. In this test the following results were measured:

Fundamental =	**-1.02 dBFSR**
2nd Harmonic =	**-59.22 dBFSR**
3rd Harmonic =	**-57.20 dBFSR**
4th Harmonic =	**-84.67 dBFSR**
5th Harmonic =	**-84.56 dBFSR**
6th Harmonic =	**-84.85 dBFSR**
SFDR =	**57.20 dBFSR**
THD(9) =	**-54.16 dBc**
SNR =	**56.99 dB**
SINAD =	**52.34 dB**



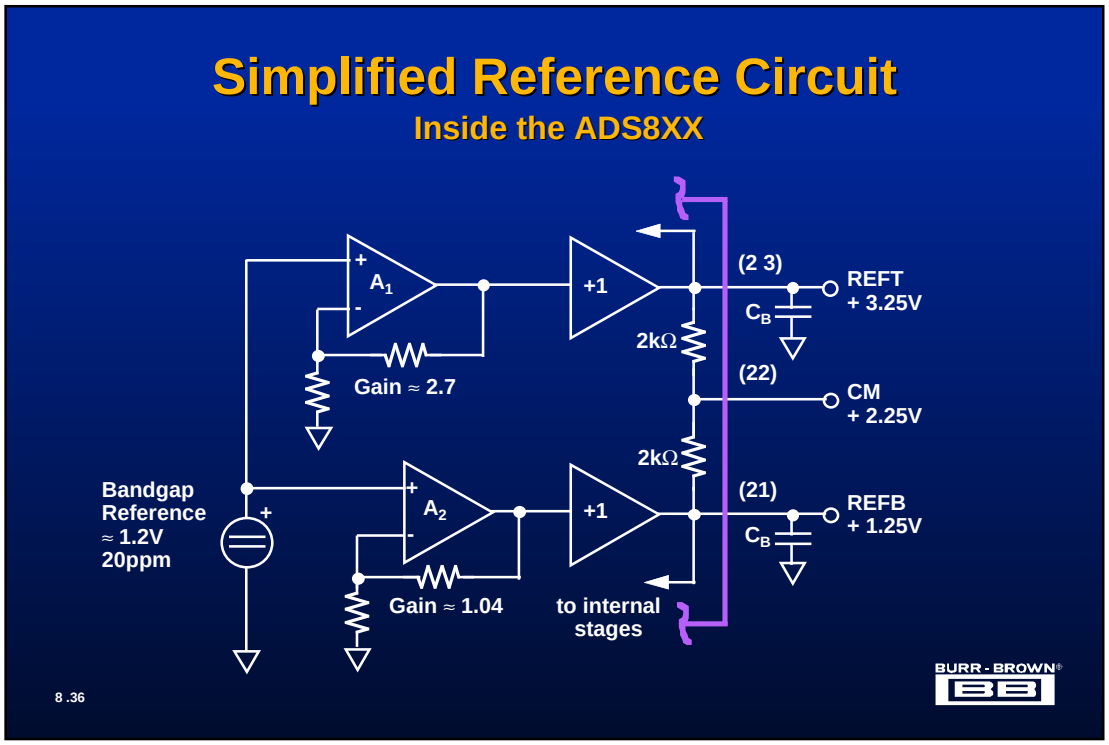
For those applications where the input signal is already available in differential form a differential in - differential out interface circuit, like the one shown here might be used. It uses the dual current feedback op amp OPA2658 which supports the low distortion performance at higher gains provided by the current feedback topology. In this particular application the op amps are set for a DC gain of +1V/V. By adding resistor R_G and capacitors C_1 and C_2 the circuit has an AC-gain that will increase as the input frequency increases. The maximum AC-gain is given by the equation $G = 1+2R_F/R_G$. The two diodes in each op amp's output serve as level shifter and are inside the feedback loops. Resistors R_1 and R_2 provide the necessary bias current for these diodes to keep them in a linear operating point. The common-mode voltage of +2.25V is added to each op amp's non-inverting input through resistors R_5 and R_6; C_3 provides some additional bypassing.

Typical component values:

R_T=25Ω, R_1=R_2=400Ω, R_3=R_4=100Ω, R_5=R_6=6kΩ, R_F=301Ω,

C_C=C_3=0.1µF, C_B=22pF, C_1=1µF, C_2=0.01µF, D_1=D_2=BAS16

1) The guaranteed minimum output swing of the OPA2658 is ±2.5V

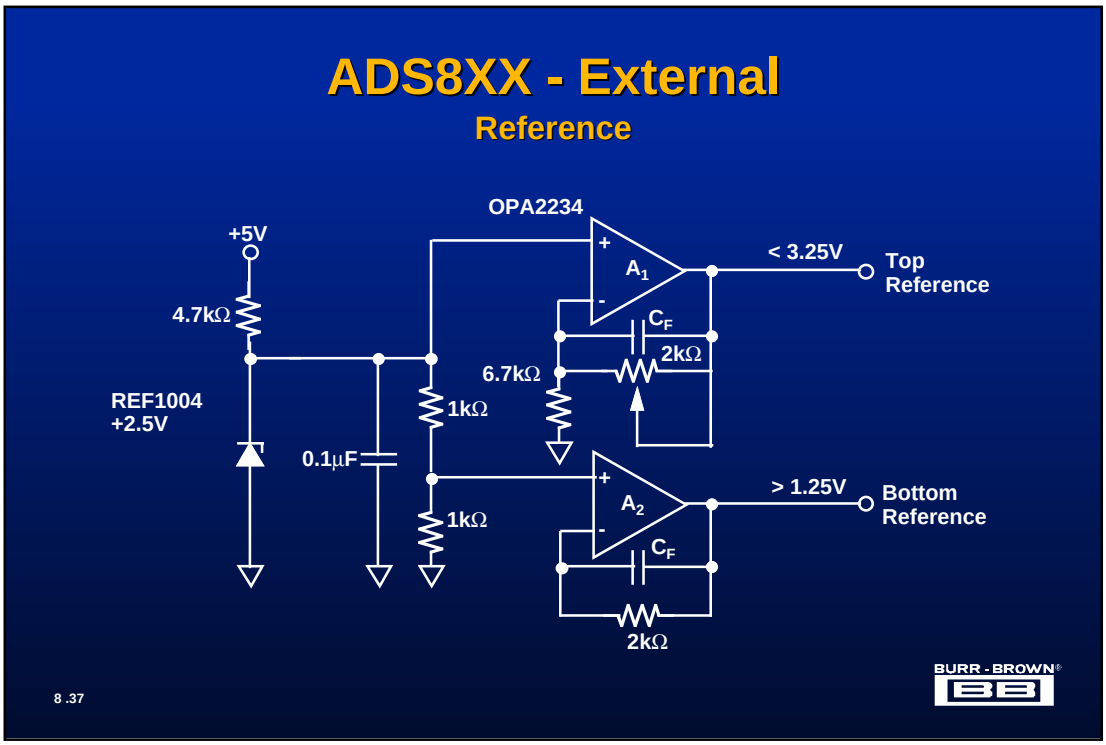


This figure depicts the reference voltage generation inside the pipeline ADCs. Because the converter have to operate on the single +5V supply voltage a common-mode level is needed to process bipolar signals. This is done by creating a common-mode mid-point, which is the center voltage of the reference voltages.

The 1.2V bandgap reference is the common source for the positive and negative reference voltage. Two amplifiers, A_1 and A_2, are set into different gains to amplify the reference voltage from +1.2V to +3.25V and +1.25V. The reference pins and the resistive divider string are driven by two buffer stages. A nominal current of about 500µA is flowing through the two 2kΩ resistors.

The common-mode pin is used to provide the common-mode voltage to the input driver circuit.

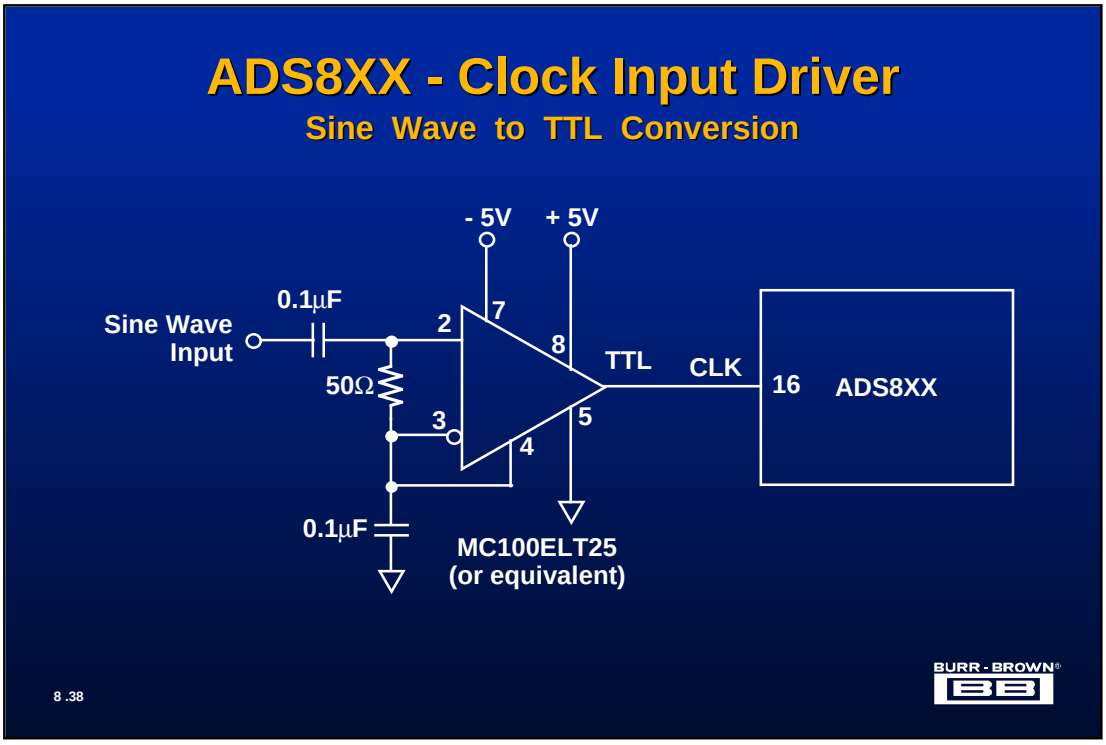
In standard operation the top (REFT) and bottom (REFB) reference pins, pins 23 and 21 respectively, should be externally bypassed with 0.1µF capacitors. This will ensure that any high frequency components at the reference points will be shunted to ground.



The internal reference buffers are limited in their output current drive to only about 1mA. As a result, these internal +1.25V and +3.25V references may be overridden by external references that have at least 10mA of output current drive capability. In this instance, the mid-scale voltage will be set halfway between the two references. This feature can be used to adjust the gain error or to change the full scale input range of the converter. The external references can vary as long as the value of the top reference is less or equal to +3.25V and the value for the bottom reference is greater than or equal to + 1.25V.

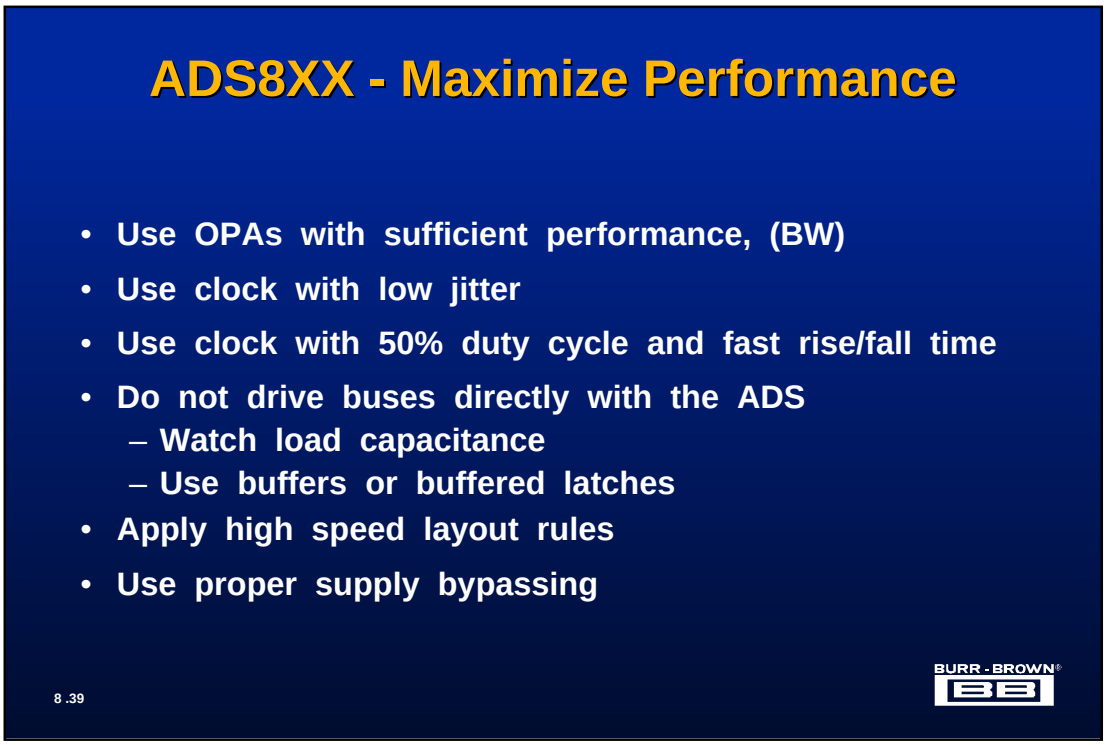
To operate with a full scale range, other than the standard 4Vp-p, the following equations can be used to calculate the required reference voltages, assuring the typical common-mode voltage of +2.25V is maintained:

$V_{refp} = 2.25V + V_{FSp\text{-}p}/4$ and $V_{refn} = 2.25V - V_{FSp\text{-}p}/4$,



A standard application problem for basically all high speed A/D converter is that they are sensitive to the convert clock quality. Clock jitter can easily become the main error source in a system and manifests itself in poor signal to noise readings. If your system exhibits SNR below expectations, the clock jitter should be investigated.

Low jitter crystal controlled oscillators usually make very good clock sources, but they only come in discrete frequency ranges. If a flexible clock source is required, usually during evaluation of the converter, the circuit shown here can be employed. This circuit, or similar using the MC10114 from Motorola, are ideal to convert from a easy available sine wave source to a low jitter TTL clock signal. The given circuit works consistently with low level inputs (0dBm), but is somewhat sensitive to jitter from the source itself. Increasing the level will help minimizing this effect. If available sine wave generators like the HP8662 or the Fluke 6080A are good choices.



Listed here are some guidelines which should help to maximize the performance when designing with the new pipelined ADS8XX converter.

If the bandwidth of the amplifier is not sufficient, the output will reflect gain errors in the signal. This bandwidth specification may be required to be a full scale bandwidth instead of a small signal bandwidth, depending on the application.

A low jitter clock enhances the accuracy of the overall signal reproduction. Furthermore, the clock should have a 50% ±5% duty cycle to insure reliable performance from the A/D converter.

Although layout has not been discussed in detail, high speed layout techniques are a must as well as sufficient power supply bypassing.

Driver Op Amp Selection Criteria

- Select op amp with distortion and noise better than ADS8XX
- Use dual op amp for better gain/phase matching
- Other important considerations:
  - Output Voltage Swing must match ADS Input
  - Single or Dual Supply System?
  - DC Accuracy/Drift if DC coupled interface
- Examine ADS for transient load currents, if any
  - Op Amp must have sufficient closed-loop bandwidth to settle to transient currents

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In order to obtain the optimal performance from the ADS8XX and the remainder of the ADS8XX product family the op amp that is used to drive the A/D converter should have better distortion and noise that the A/D converter. When differential inputs require that two op amps be used, a dual op amp will offer better matching over temperature than two singles in separate packages. Additionally, the output voltage swing of the op amps should accommodate the maximum input of the A/D converter in order to achieve full dynamic range performance. Although the ADS8XX family is a single, 5V supply family, dual supplies are often required to power the op amps in the input drive circuitry.

As a final note, the transient response of the driver circuitry can have a significant affect on the perceived performance of these high speed converters. The bandwidth should be sufficient as to not to cause attenuation at higher frequencies due to gain distortion and the transient currents and voltages at the output of the amplifiers should sufficiently settle before the A/D converter is instructed to sample its input signal.

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