HEWLETT® PACKARD

IrDA Data Link Design Guide

Introduction

Welcome to the World of Infrared Data Communications! This guide is designed to provide you with the background necessary to design and implement your very own IrDA compatible data link. Within these pages, you will find detailed information on all phases of the design process, from architectural considerations through board layout. You will also learn about the Infrared Data Association (IrDA) — about it's purpose, and about the IrDA specification for IR data transfer.

In addition to the information presented here, there is much more information available from the sources listed in the References. In particular, be sure to check the HP IR Web Site or the Fax Back Service, where you will find the most recent Data Sheets and Application Notes.

References

Hewlett-Packard

Components Sales Response Center:

Americas/ Canada	(800) 235-0312 or 408-654-8675
Far East/ Australasia	Call your local HP sales office.
Japan	(81 3) 3331 6111
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For product Data Sheets and Application Notes:

Fax Back Service (North America only)	(800) 450-9455
World Wide Web	http://www.hp.com/go/ir

Infrared Data Association (IrDA)

Phone	(510) 943-5600
World Wide Web	http://www.irda.org/

Support Hardware

National Semiconductor	(800) 272-9959 http://www.nsc.com
VLSI Technology	(888) 857-4347 http://www.vlsi.com
Standard Microsystems	(516) 435-6000 http://www.smc.com

References, continued

Support Software

Counterpoint Systems Foundry	(541) 757-1486 http://www.countersys.com
Genoa Technology	(805) 531-9030 http://www.gentech.com
Microsoft Corporation	(800) 426-9400 http://www.microsoft.com
Parallax Research	+65 665-6938 http://www.parallax-research.com
Puma Technology	(408) 987-0200 http://www.pumatech.com
Travelling Software	(206) 483-8088 http://www.travsoft.com
Connexus	(510) 490-8003

Other

General Electric Plastics	(800) 845-0600

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The IrDA Specification

This section presents an overview of IrDA, and the features and requirements of IrDA compliant products.

Overview

The Infrared Data Association (IrDA) is an independent organization whose charter is to create standards for interoperable, low cost IR data interconnection. IrDA devices provide a walk-up, point-to-point method of data transfer that is adaptable to a broad range of computing and communicating devices. Setting standards for IR communication is key to effortless communication between various types and brands of equipment. It is the goal of IrDA to set standards and protocols which can be reasonably and inexpensively implemented in order to promote the proliferation of IR communication. The first version of the IrDA specification, Version 1.0, provided for communication at data rates up to 115.2 Kb/s. Version 1.1 extended the data rate to 4 Mb/s, while maintaining backward compatibility with Version 1.0 products.

Without a communication protocol, such as that provided by IrDA, a non-cabled link is inherently not robust. Unlike a cable, which is semi-permanently attached, the ends of an IR link may move freely within range and out of range The link may even be broken in the middle of a transmission. IrDA defines a set of specifications, or protocol stack, that provides for the establishment and maintenance of a link so that error free communication is possible. The IrDA Standard includes three mandatory specifications: the Physical Layer, Link Access Protocol (IrLAP), and Link Management Protocol (IrLMP).

While the primary focus of this guide is implementation of the Physical Layer, we will start with a brief overview of the software protocols. Further information about IrDA, as well as the specifications themselves, are available directly from IrDA (see References, page iii.)

IrDA Protocol Stack

The IrDA specifications provide guidelines for link access (IrLAP), link management (IrLMP), and for the electrical-optical hardware interface(Physical Layer). The protocol is arranged as a stack, where data from application programs are passed down through the stack and eventually transmitted as light pulses. See Figure 1. IrLAP and IrLMP are the two software layers of the protocol that are required in addition to the physical layer.

The first layer above the physical layer is the Link Access Protocol (IrLAP). This layer is an IR adaptation of the HDLC (High-level Data Link Control) protocol. The function of the IrLAP layer is to support link initialization, device address discovery and conflict resolution, connection startup, data exchange, disconnection and link shutdown. IrLAP specifies the frame and byte structure of IR packets as well as the error detection methodology for IR communication.

The layer above IrLAP is the Link Management Protocol, or IrLMP. Within the link connection provided by IrLAP, link functions and applications are managed by IrLMP software. IrLMP assesses the equipment and services available on the connected pieces of equipment, and manages negotiation of parameters such as data rate, number of BOFs (beginning of frame), and link turn around time. IrLMP then manages the correct transfer of data and information.

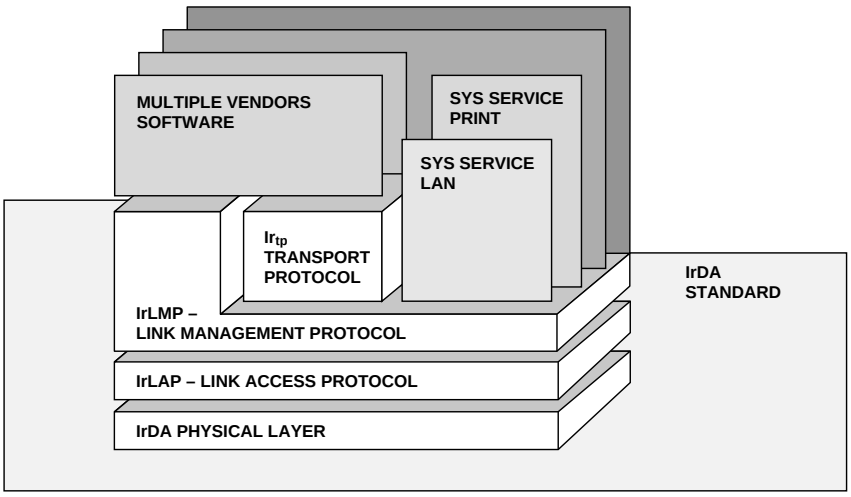


Figure 1. IrDA Protocol Stack.

Software Support
Many implementations of the IrDA architecture are supported on PCs by Windows 95. In addition, IrDA drivers have been written for a number of microcontrollers. A number of vendors also provide the service of writing drivers and application software. Please see the Reference list (page iii) or contact IrDA for specific names of vendors.

IrDA Physical Layer

Overview
The Physical Layer Specification provides guidelines for the connection of equipment using IR. The specification is designed to guarantee error free communication from a distance of 0 cm to 1 meter, at an off axis angle of 0 to at least 15 degrees (Figure 2). Included are specifications for modulation, viewing angle, optical power, data rate, and noise immunity in order to guarantee physical interconnectivity between various brands and types of equipment. The specifications also ensure successful communication in typical environments where ambient light or other IR noise sources may be present, and minimize interference between IR participants.

The specifications for optical intensity for the transmitter and sensitivity for the receiver were chosen to guarantee that the link will work from 0 cm to 1 meter. Receiver sensitivity was chosen so that a minimum intensity emitter will still be seen at 1 meter, and a maximum intensity emitter will not saturate the receiver even at 0 cm.

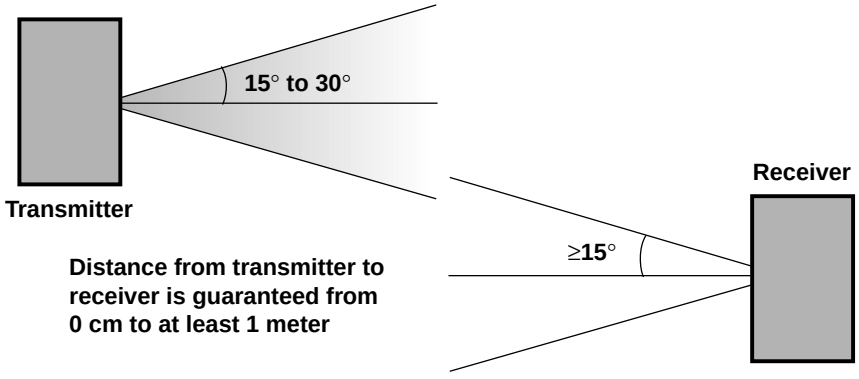


Figure 2. IrDA Viewing Angle and Distance.

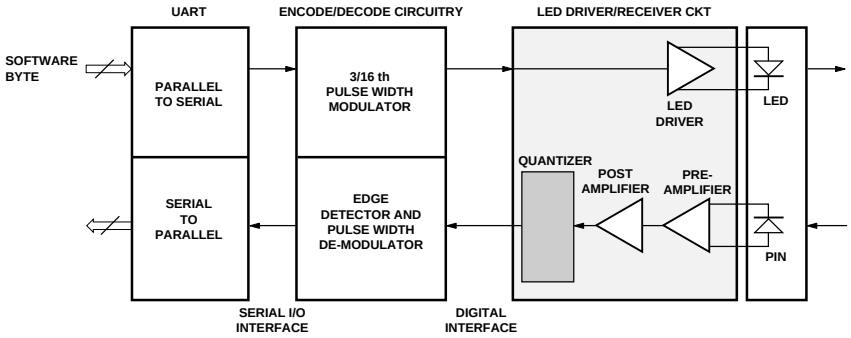


Figure 3. IrDA Version 1.0 Physical Layer Block Diagram.

IrDA data rates range from 2.4 Kb/s to 4 Mb/s. Link data rate is negotiated when the link starts up. IrDA requires that a link always start up at 9.6 Kb/s, but then allows the link to negotiate higher (or lower) data rates if supported by both ends. Data rates of less than 4 Mb/s use a RZI (return to zero, inverted) modulation, and the 4 Mb/s data rate uses a 4 PPM (pulse position) modulation Both of these modulation techniques are described in more detail below.

115.2 Kb/s Data Rate
Figure 3 shows a block diagram of the physical layer for data rates up to 115.2 Kb/s. This was conceived as a link that would work readily with conventional UARTs, such as the 16550. As such, it is a straightforward extension of the serial port. Note in Figure 3, however, that the data is first encoded before being transmitted as IR pulses. This is required because UARTs and serial ports use NRZ (non return to zero) coding where the output is the same level for the entire bit period and can stay at one level for multiple bit periods. This can be seen in Figure 4 as the data labeled UART frame. This is not optimal for IR data transfer since a continuous string of bits could turn on the LED transmitter for an arbitrarily long time. Thus the power in the LED would need to be limited, which would limit working distance. Instead, IrDA requires pulsing the LED in a RZI (return to zero, inverted) modulation scheme so that the peak to average power ratio can be increased. IrDA requires the maximum pulse width to be 3/16 of the bit period. The minimum pulse width can be as little as 1.41 us, which is derived from 3/16

of the highest data rate of 115.2 Kb/s. The effect of the encoding can be seen in Figure 4 as the data labeled IR Frame. A 16x clock is conveniently available on many UARTs, so it is easy to count 3 clock cycles to encode the transmitted data, and to stretch the received data with 16 clock cycles. Note that this scheme requires an encoder/decoder (endec), either embedded in the I/O chip or as a discrete component. This is discussed in more detail in the chapter on Architectural Options, beginning on page 6.

4 Mb/s Data Rate

Version 1.1 of the IrDA Specification extended the data rate to 4 Mb/s while retaining compatibility with legacy (Version 1.0) products. This is possible because all links are required to start at 9.6 Kb/s and negotiate to higher data rates if both ends support them. Thus, a product capable of 4 Mb/s must still work at 9.6 Kb/s. IrDA only requires that links work at 9.6 Kb/s — all higher data rates are optional. Thus, the 4 Mb/s-capable device will communicate with a device that only supports 9.6 Kb/s.

A 4 Mb/s IrDA link uses a modulation scheme known as 4 PPM (Pulse Position Modulation), instead of the 3/16 modulation used for slower data rates. With 4 PPM, information is conveyed by the position of a pulse within a time slot.

Bit Pattern	Pulse Position
00	1000
01	0100
10	0010
11	0001

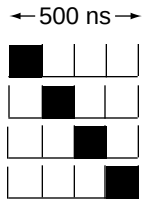


Figure 5. 4 PPM Modulation.

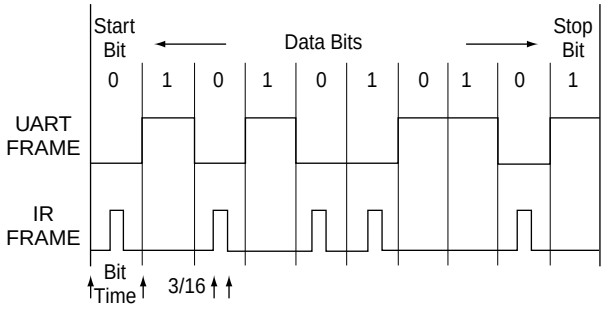


Figure 4. IrDA Data Modulation (3/16).

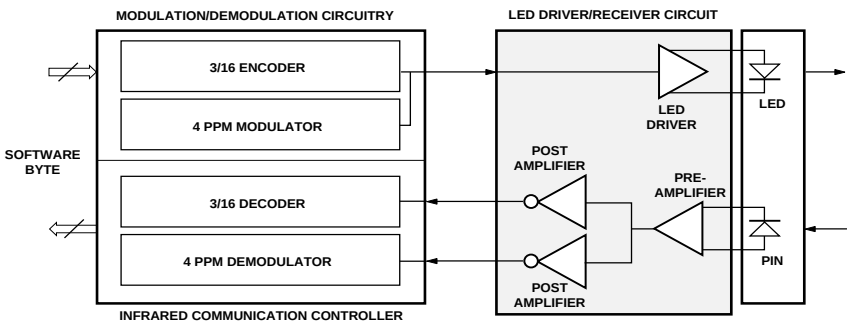


Figure 6. IrDA Version 1.1 Physical Layer Block Diagram.

In the 4 PPM scheme (Figure 5), two data bits are combined to form a 500 ns "data bit pair" (DBP). This DBP is divided into four 125 ns time slots, or "chips". The two bits to be encoded will have one of 4 states: 00, 01, 10, 11. Depending upon which of these states is present, a single pulse is placed in either the first, second, third or fourth 125 ns time slot. Thus, a demodulator, after phase locking on the incoming bit stream, can determine the data pattern by the location of the pulse within the 500 ns time period. The demodulator phase locks with a string "preamble" fields. A preamble consists of 16 bits, and is transmitted 16 times.

The block diagram for the Ver. 1.1 4 Mb/s Physical Layer (Figure 6) looks similar to the Ver. 1.0 block diagram, except that the UART and the Encode/Decode circuitry are replaced with an I/O device that is designed for 4 Mb/s IrDA data communication. This device does the encoding and decoding of both the 3/16 and the 4 PPM modulation.

1.152 Mb/s and 576 Kb/s Data Rates

The intermediate data rates of 576 Kb/s and 1.152 Mb/s are also supported by IrDA. These use an RZI modulation similar to the 3/16 modulation used at 115.2 Kb/s and slower, but use a nominal 25% pulse width. Consult the IrDA physical layer specification for more information on this topic (see References).

Key Physical Layer Parameters

The IrDA physical layer specification defines the requirements for a serial, half-duplex IR link that will communicate with another IrDA device at distances from

0 cm to 1 meter. The key physical layer parameters are shown in Table 1.

Please see the Hewlett-Packard Application Note, "Evaluation of Infrared Transceivers for IrDA Compliance."

Table 1. Key IrDA Physical Layer Parameters.

ACTIVE OUTPUT (TRANSMITTER) SPECIFICATIONS	Data Rates	Minimum	Maximum
Peak Wavelength, Up, um	All	0.85	0.90
Maximum Intensity In Angular Range, mW/sr	All	—	500
Minimum Intensity In Angular Range, mW/sr	115.2 kb/s and below Above 115.2 kb/s	40 100	— —
Half-Angle, degrees	All	±15	±30
Rise Time Tr & Fall Time Tf, 10-90% , ns	115.2 kb/s and below Above 115.2 kb/s	— —	600 40
Optical Over Shoot, %	All	—	25
Signaling Rate and Pulse Duration		See IrDA Spec	See IrDA Spec
Edge Jitter, % of nominal bit duration	115.2 kb/s and below	—	±2.3
Jitter Relative to Reference Clock, % of nominal bit duration	0.576 and 1.152 Mb/s	—	±2.9
Edge Jitter, % of nominal chip duration	4.0 Mb/s	—	±4.0
ACTIVE INPUT (RECEIVER) SPECIFICATIONS			
Maximum Irradiance In Angular Range, mW/cm^2	All	—	500
Minimum Irradiance In Angular Range, $\mu W/cm^2$	115.2 kb/s & below Above 115.2 kb/s	4.0 10.0	— —
Half-Angle, degrees	All	±15	—
Receiver Latency Allowance, ms	All	—	10
LINK INTERFACE SPECIFICATIONS			
Minimum Link Length, m	All	0	0
Maximum Link Length, m	All	1	-
Bit Error Ratio, BER	All	—	10^{-8}
Receiver Latency Allowance, ms	All	—	10

Optical
Figures 7 and 8 show the IrDA requirements for output intensity and input irradiance vs. angle. For the output (Figure 7), the intensity must be between the minimum and the maximum everywhere within a cone with a half angle of 15 degrees off the optical axis, and must fall below the minimum at angles greater than 30° off the optical axis. For the optical input (Figure 8), the receiver must be able to recognize a signal between the minimum irradiance (depending upon data rate, per Table 1) and the maximum of 500 mW/cm^2, anywhere within a cone with a half angle of 15° with respect to the optical axis.

Half-Duplex and Latency
The IrDA link is half-duplex, and there is a time delay allowed from when a link stops transmitting until when it must be ready to receive. The IrDA link cannot send and receive at the same time because the transmitter and receiver are not optically isolated, so the transmitted signal would interfere with the incoming signal. When the transmitter is emitting light it may even saturate its own receiver, and disable it from receiving data from another source. IrDA allows a period of 10 ms after finishing transmitting for the receiver to regain its full sensitivity. Shorter times may be negotiated when the link starts up. This delay, from the time the transmitter stops sending light pulses to the time the receiver is guaranteed ready to receive data, is called latency. Latency is also known as receiver set-up time.

Ambient Light
In order for the IrDA link to work under a wide range of environmental conditions, there are requirements for rejection of ambient noise. IrDA specifies the test methods for measuring the data integrity of the link under electromagnetic fields, sunlight, incandescent lighting and fluorescent lighting. An IrDA receiver must be able reject up to 10 klux of sunlight, 1000 lux of fluorescent light and 1000 lux of incandescent light. These values were chosen as typical of what may be encountered under normal use conditions. Please refer to the IrDA Physical Layer Test Specification for test methodologies.

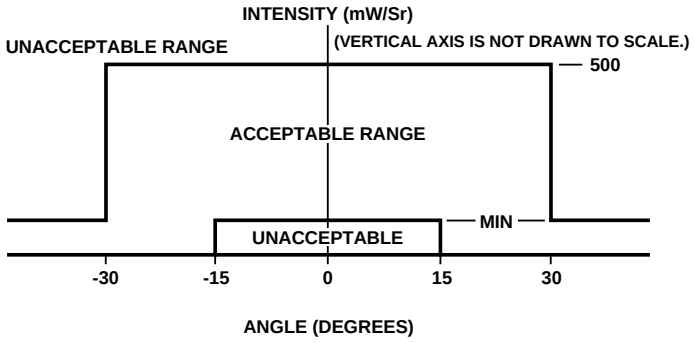


Figure 7. Acceptable Optical Output Intensity Range.

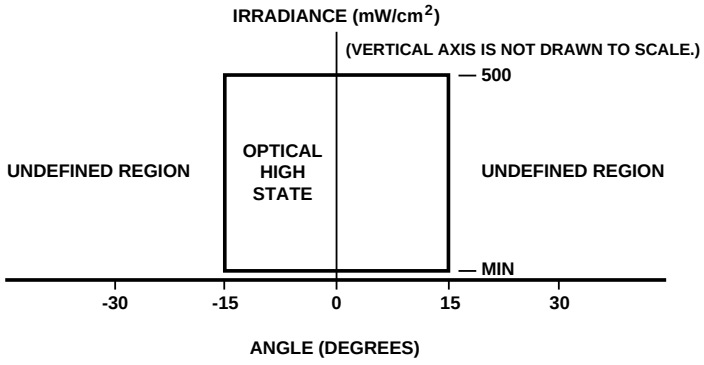


Figure 8. Optical High State Acceptable Range.

Hewlett-Packard Patent Information

HP owns the patent (# 5,075,792) for the section of the physical layer that encodes, receives and decodes the data. A patent license (licensed through IrDA) is required for manufacturers of components that are covered by the patent. Users of licensed components have the license rights passed through to them. For more information, contact IrDA (see References).

Architectural Options

This section presents a number of system architectures and typical products for which they are appropriate. Choosing an architecture is where an IrDA design begins.

Typical Architectures

As mentioned above, the Ver 1.0 IrDA architecture was intended to work with a serial port on a conventional UART. To achieve this, a number of design approaches are possible, but will vary slightly based on where the serial data comes from and where the encoding is done. A number of vendors now offer I/O chips with the IrDA encoding and decoding built in.

Typical architectures will usually fall into one of the categories described below. The architecture described below most similar to the block diagram in Figure 3 in the preceding chapter is the UART with Endec (Figure 11), while the easiest to implement in a system are the "Super I/O" and 4Mb I/O architectures (Figures 9 and 10). For specific device recommendations, please refer to the Application Note, "IrDA Physical Layer Implementation for Hewlett-Packard's Infrared Products."

2.4 Kb/s to 115 Kb/s Super I/O (Figure 9)

Typical Application: Notebook and Desktop PCs

Most PC systems, which typically have a broad range of I/O requirements, can utilize a "Super I/O" chip. In addition to a UART with IrDA encoding and decoding built in, these chips are also able to control the floppy disk drive, hard disk drive, parallel port, keyboard, modem, and more.

The serial IR output and input of these Super I/O chips connect directly to the input and output of HP's 115.2 Kb/s IR transceivers, with no support logic required. For any I/O chip, the Configuration Register bits must be set so that the I/O chip is set to operate in the proper modes. The settings should be Half-Duplex, IrDA, SIR, transmit active high, and receive active low. UART2 is usually enabled by the bit settings.

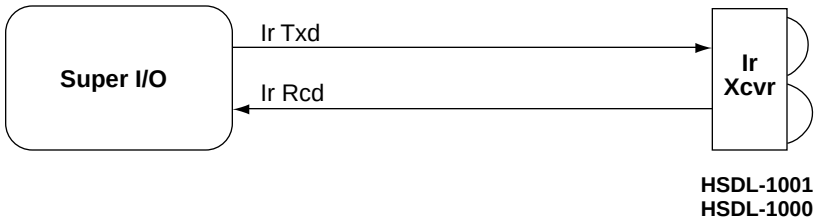


Figure 9. Super I/O Interface (2.4 Kb/s to 115.2 Kb/s).

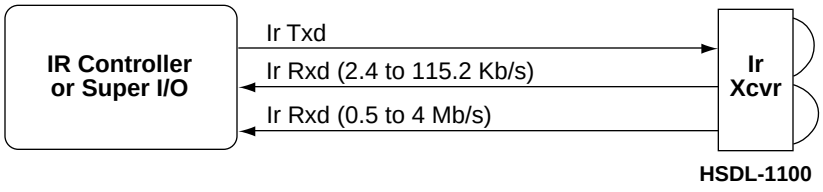


Figure 10. 2.4 Kb/s to 4 Mb/s.

Some I/O chips require that the transmit signal be AC coupled to the transceiver module to prevent setting the output in a DC "on" state at power-up. Please refer to the Application Note, "IrDA Physical Layer Implementation for Hewlett-Packard's Infrared Products" for details.

These Super I/O chips are made by various semiconductor manufacturers including National Semiconductor and Standard Microsystems Corporation (SMC). Please see the Application Note, "IrDA Physical Layer Implementation for Hewlett-Packard's Infrared Products" for specific device recommendations.

2.4 Kb/s to 4 Mb/s (Figure 10)

Typical Application: Notebooks, Printers or other with ISA or PCI Bus

Since a 115.2 Kb/s link, as defined by Version 1.0 of the IrDA Physical Layer Specification, was designed to work with a conventional UART, it was limited to the maximum data rate supported by the UART, which is 115.2 Kb/s. The Version 1.1 specification extends the data rate to 4 Mb/s. This makes it necessary to have an I/O interface different from a conventional UART, and also requires a different modulation scheme.

The block diagram for a 4 Mb/s Physical Layer looks similar to Figure 3, except that the UART and the Encode/Decode circuitry are replaced with an I/O device that is designed for 4 Mb/s IrDA data communication. Since all IrDA links are required to start up at 9.6 Kb/s (with 3/16 modulation), this device does the encoding and decoding for the 115.2 Kb/s (3/16

modulation) channel as well as the 4 Mb/s (4PPM modulation) channel. A number of I/O chips that connect to the ISA bus as well as the PCI bus are available. Please refer to the Application Note, "IrDA Physical Layer Implementation for Hewlett-Packard's Infrared Products" for a listing of I/O devices and recommendations for interfacing with them.

Note: All of the following architectures operate up to a maximum data rate of 115.2 Kb/s.

16550-type UART, Microcontroller or Embedded I/O with 16x Clock (Figure 11)

Typical Application: PDAs, Industrial Controllers, Analytical Instruments

Many electronic machines such as PDAs, Industrial Controllers, and Analytical Instruments may use a 16550 or similar UART for the I/O interface, or have the UART embedded into an ASIC. As seen in Figure 12, the UART's TXD output is an NRZ (non-return to zero) signal that is 100% duty-cycle (full bit width). This signal must be modulated before transmission, and demodulated (stretched) when received.

A discrete Encoder/ Decoder (Endec) chip, such as the HSDL-7000 is used to modulate the data. Figure 12 shows how the HSDL-7000 has an IrTXD output that is 3/16 of the bit period (3 of 16 clock cycles). The 16x Clock is typically available as a UART output, and is usually called Baudout.

In Figure 13, the received pulse (IrRXD) is stretched by the Endec to the width of 16 clock pulses, or the original bit period. The clocks at both ends of the link do not need to be synchronized, but do need to be at the same frequency, as determined at link startup.

For system designers who prefer to embed IrDA communications in an ASIC, Hewlett-Packard will provide the IrDA Ver. 1.0 Endec Netlists at no charge. This may be useful for system designers who do not require the functionality of a full Super I/O chip, and who do not wish to use a discrete UART. With the IR encode/ decode function incorporated into the system ASIC, it can then interface directly with the IR transceiver module. Please refer to the Application Note, "IrDA Physical Layer Implementation for Hewlett-Packard's Infrared Products."

Note that the IrDA transceivers are designed specifically for modulated data and will not work in NRZ mode. This is due to the fact that the receiver generates an output pulse (RXD) for each incoming IR pulse. The width of the receiver's RXD output pulse is typically not more than 20 us, regardless of the width of the IR input pulse. Thus, a continuous string of "1" bits (in NRZ coding) would look like one single incoming bit, and thus would be erroneously translated to just one pulse at the transceivers output.

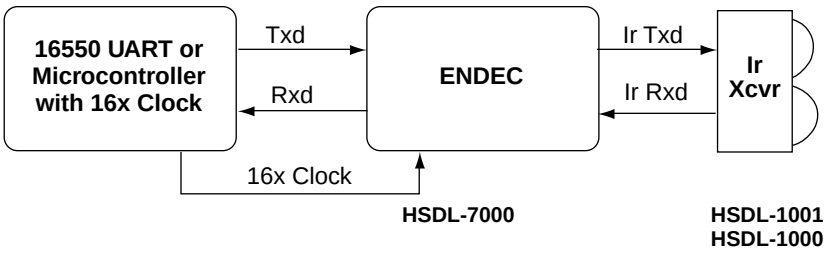


Figure 11. 16550-Type or Embedded UART with 16x Clock.

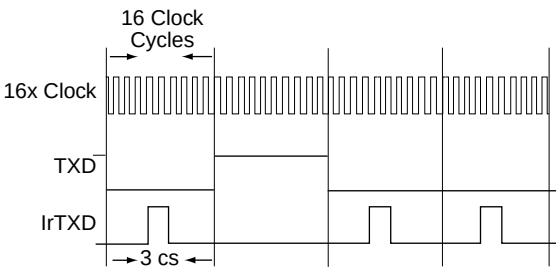


Figure 12. Ir Transmit.

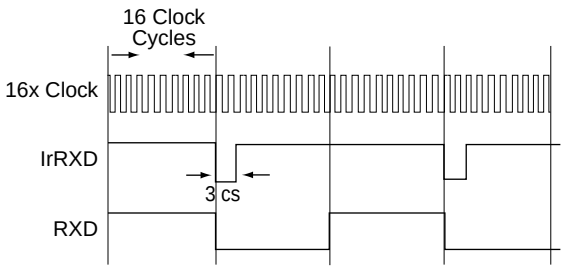


Figure 13. Ir Receive.

UART, Microcontroller, or Embedded I/O without Clock (Figure 14)

Typical Application: Custom I/O, Portables, some Microcontrollers

In some systems, a 16x clock for the Endec may not be provided by the system, and must be generated. As mentioned earlier, IrDA only requires that a link operate at 9.6 Kb/s. Thus, a clock for a system that runs only at 9.6 Kb/s need only provide a fixed frequency clock that runs at 16 times 9600, or 153600 Hz. A system that needs to go faster will need a means of changing the data rate and thus programming the clock. This can be done with either the HSDL-7000 and some external circuitry, or with the HSDL-7001, which has an internal programmable oscillator. In either case, the oscillator is typically programmed with RS232 lines that are not used in an IR link, such as RTS and DTR, or others. Such a system would need software drivers to correctly configure the programming signals to convey baud rate information. Please see the references for suppliers of software drivers.

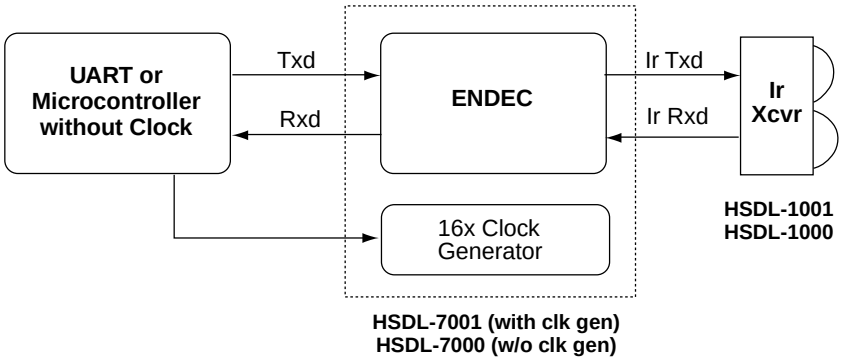


Figure 14. UART, Microcontroller, or Embedded I/O without Clock.

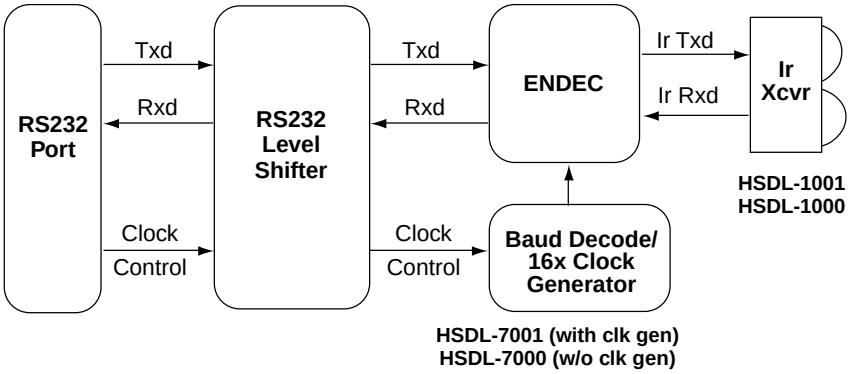


Figure 15. RS232 Adapter.

Interface to RS-232 Port (Figure 15)

Typical Application: Add IR Functionality to RS232 Port

Some IR ports may be designed to work with existing products and communicate through the RS232 port, or designed as external IR adapters. In these cases, the architecture is similar to Figure 14, where the data needs to be encoded but no clock is available. As above, the clock will need to be generated in the IR adapter, and to go faster than 9.6 Kb/s, will require a programmable clock. Also, the voltage levels need to be shifted from RS232 levels back to logic levels using one of the commercially available RS232 interface circuits. Finally, sufficient power must be provided so that the peak pulsed LED forward current is available to the transmitter while sending data. The average current will be I_f (from data sheet) * 3/16 * (percentage of 0s in the data stream). At data rates slower than 115.2 Kb/s, the pulse width may be fixed at 1.6 µs instead of 3/16 of the data rate to reduce average current.

Hewlett-Packard Products

Having selected an architecture, the IrDA system designer can now select the proper components and develop the circuit diagram.

Hewlett-Packard manufactures a broad selection of products that may be used to implement a variety of IrDA designs. Please refer to the HP Infrared Components Selection Guide for an overview of these products. This section will describe the characteristics of these various components. Please see the Data Sheets or Product Catalog (see References) for specific parametric information.

Integrated Transceiver Modules

115.2 Kb/s Transceiver
The HSDL-1001 (see Figure 16) is an integrated 115.2 Kb/s transceiver, and is designed to perform the fully IrDA compliant IR transmit and receive functions for the system. The transmitter converts the 3/16th bit width electrical pulses from the I/O chip or endec into IR light pulses. The receiver detects IR light pulses and converts them to TTL level electrical pulses.

The integrated design of the HSDL-1001 enables ease of implementation and ease of compliance to all IrDA physical layer specifications. It includes the optics, LED with buffered LED driver, and PIN photodiode and Receiver circuits in one package. The design of the transmitter guarantees the intensity and viewing angles required by IrDA, while the receiver circuitry enables data transfer at guaranteed link distances from 0 cm (nose to nose) to at least 1 meter, even in the presence of ambient electrical and optical noise.

The HSDL-1001 is guaranteed to meet all IrDA specifications over operating temperature, supply voltage and life of the part. All electrical specifications are also guaranteed over temperature, voltage and lifetime. Supply voltage range is over the full range from 2.7 V to 5.5 V. The devices feature an idle supply current (while ready to receive) of only 200µA (typical), and the ability to shut the part down to only 5 µA (typical) for further supply current savings.

Transmitter
The transmitter uses a high speed, high efficiency TS AlGaAs LED, along with a high speed drive circuit to produce high power IR pulses with minimal pulse width distortion. The transmitter features a buffered input to reduce input current to typically 40 µA so it can be driven directly by CMOS logic. The efficiency of the LED and the optical design of the package guarantee IrDA minimum light intensity at a drive current of 240 mA. The speed of the LED and drive circuitry minimize the rise and fall times of the LED signal edges, improving the detection capability of the corresponding IR receiver.

The transmitted radiant intensity (Ie) at 240 mA LED current is guaranteed to be at least 44 mW/sr over the operating temperature range and supply voltage range, and over the normal operating life of the transceiver module. The guaranteed intensity of 44 mW/sr allows an additional 10% guardband for the system's cosmetic window loss, while still enabling the IrDA minimum of 40 mW/sr out of the system.

The transmitter uses a few external passive components. The choice of these components is

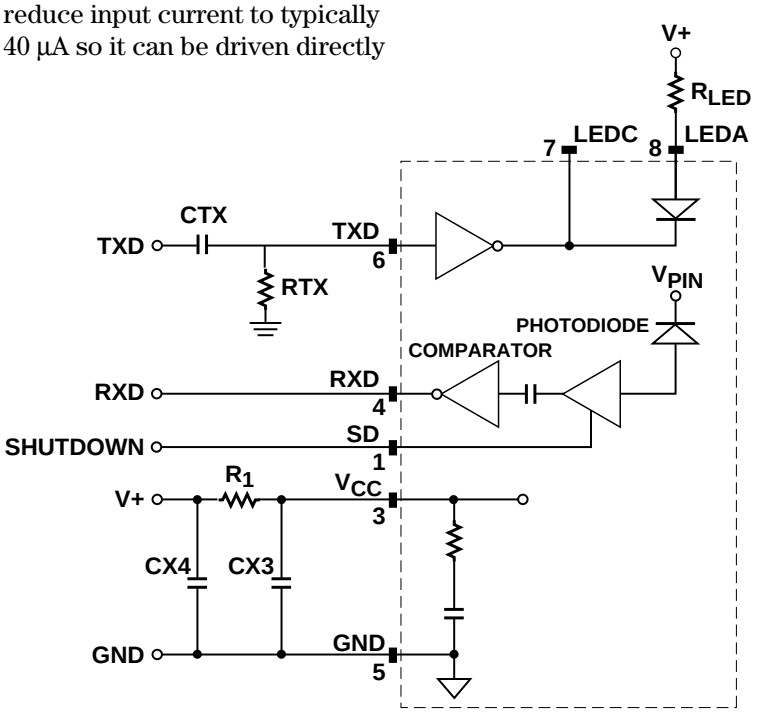


Figure 16. HSDL-1001 115.2 Kb/s Transceiver.

described in the chapter entitled Design Guidelines. RLED is the LED current limiting resistor. Its value is chosen based upon supply voltage and desired current, and is typically in the range from 0.8 to 10 ohms. RTX and CTX AC couple the input, and are only required when the input can go high for longer than 90 us, such as when some Super I/O chips are used.

Receiver
Dynamic Range: The wide dynamic range, over 5 orders of magnitude, required by the IrDA physical layer specification necessitates adjustment of the receiver threshold to incoming signal levels. The HSDL-1001 uses feedback and limiting within the first stage amplifier circuitry to adapt to incoming signal levels. The amplifier design allows maximum sensitivity for low power signals (4 $\mu W/cm^2$) and also limits pulse width distortion for high power signals (500 mW/cm^2). The performance of the HSDL-1001 receiver eliminates the need for any additional AGC (automatic gain control) circuitry.

AGC circuitry can be used in an IR receiver to obtain wide dynamic range. The presence of AGC circuitry is not a guarantee that the IrDA specifications will be met. Some implementations using AGC circuitry have been shown to lead to bit errors at large signal levels (short IR link distances). The complete IR system should be tested for IrDA compliance at both short (nose-to-nose) and long (1 meter) distances regardless of the design methodology used to obtain wide dynamic range.

Power Supply and EMI Noise: Any IR transceiver implementation requires special attention to EMI and Power Supply noise. The analog functions (IR detector and pre-amplifier) are very sensitive, and thus require more attention to EMI and power supply noise than typical digital integrated circuits. Noise immunity is the maximum amount of noise that the receiver can sense before exceeding a 10^{-8} bit error rate. Noise levels above the noise immunity will effectively reduce the receiver sensitivity and therefore the IR link distance. All IR transceiver solutions require improved ground plane design and capacitive decoupling over standard practices for digital integrated circuits. See the section on Board Layout Guidelines (page 16) for low noise design techniques.

The HSDL-1001 exceeds the IrDA specification for EMI Immunity when board layout is implemented according to the board layout section of this design guide. The EMI Immunity is greater than 200 volts/meter for any square wave noise source, and even higher for sinusoidal noise sources. For example, a 10 volt peak-peak square wave signal source placed 5 cm from the transceiver module would produce EMI of 200 volts/meter.

The HSDL-1001 offers improved supply noise rejection over previous circuits. It is recommended that the noise voltage at the Vcc pin be less than 75 mV. The external components CX3 and CX4 are power supply bypass capacitors, and are used to reduce noise at the Vcc pin. A power supply filter resistor, R1 may be optionally added if required to further increase supply noise rejection. The choice of these components is described in the chapter entitled Design Guidelines.

Ambient Light: The HSDL-1001 IR transceiver module makes use of several technologies to reduce the interfering effects of ambient sunlight, incandescent light or fluorescent light. The package mold compound is tinted with dye to filter out visible wavelengths. The lens of the detector is designed to "see" light only within the IrDA viewing angle and exclude light from outside of that angle. The first stage amplifier of the receiver contains daylight cancellation circuitry to eliminate the ambient light portion of incoming signals, and the amplifier is bandwidth limited to reject signals out of the IrDA band. Using these techniques, HP can ensure robust performance under IrDA specified ambient light conditions.

4 Mb/s Transceiver
The HSDL-1100 (see Figure 17) is a fully integrated 4 Mb/s transceiver module, and is designed to perform the IR transmit and receive functions for the system from 2.4 Kb/s to 4 Mb/s. It comes in a package similar to the HSDL-1001, with improved thermal characteristics to allow the increased LED current required to achieve the 100 mW/sr transmitted LED power required for signaling at 0.576 Mb/s and above. The HSDL-1100 is specified over the supply voltage range from 4.5 V to 5.5 V.

Transmitter
The transmitter uses a high speed, high efficiency TS AlGaAs LED to produce an IR signal of the intensity and speed required by IrDA. The LED drive transistor is Schottky clamped to aid in meeting the IrDA optical transition time and pulse width requirements for 4 Mb/s signaling. The external components CX2 and R1 are recommended to obtain current peaking, which creates faster optical edges and minimized pulse width distortion. Fast optical edges increase the link distance by effectively increasing the power budget of the overall IR link.

Receiver
The receiver consists of two channels, RXD-A (2.4-115.2 Kb/s) and RXD-B (0.576-4 Mb/s). Both channels use the same detector and pre-amplifier stage. Both channels use CX1, CX5, CX6, and R3 to filter out power supply noise. The RXD-B channel uses an adaptive threshold circuit to maximize the data eye opening for any signal level within the IrDA required dynamic range. The RXD-B channel also uses a squelch circuit to eliminate chatter on RXD-B when no IR signal is present. The adaptive threshold and squelch circuits use CX3 and CX4.

In general, 2.4-115.2 Kb/s received IR signals create output pulses on RXD-A, and 0.576-4 Mb/s IR signals create output pulses on RXD-B. However, IR signals in the 100 kHz – 1 MHz range may appear on both RXD-A and RXD-B, depending on the IR signal strength. The presence of a signal at both RXD-A and RXD-B should not be a problem since the I/O chips are designed to look at only one channel at time. The channel that is enabled is based upon the data rate that is selected by the software when the link is started.

Dynamic Range: The dynamic range required of the receiver by IrDA for a 1 meter link is 4 μW/cm^2 to 500 mW/cm^2 for 2.4 to 115.2 kb/s, and 10 μW/cm^2 to 500 mW/cm^2 for 0.576 to 4 Mb/s. The wide dynamic range requires a special circuit which adjusts to the signal level for comparison to a threshold. The adaptive threshold circuit quickly adapts to the incoming signal level and eliminates the need for any external AGC circuitry or adjustment.

Power Supply and EMI Noise: Any IR transceiver implementation requires special attention to EMI and Power Supply noise. The analog functions (IR detector and pre-amplifier) are very sensitive, and thus require more attention to EMI and power supply noise than typical digital integrated circuits. Noise immunity is the maximum amount of noise that the receiver can sense before exceeding a 10^{-8} bit error rate. Noise levels above the noise immunity will effectively reduce the receiver sensitivity and therefore the IR link distance. All IR transceiver solutions require improved ground plane design and capacitive decoupling over standard practices for digital integrated circuits. See the section on Board Layout Guidelines (page 16) for low noise design techniques.

The HSDL-1100 exceeds the IrDA specification for EMI Immunity when board layout is implemented according to the board layout section of this design guide. The EMI Immunity is

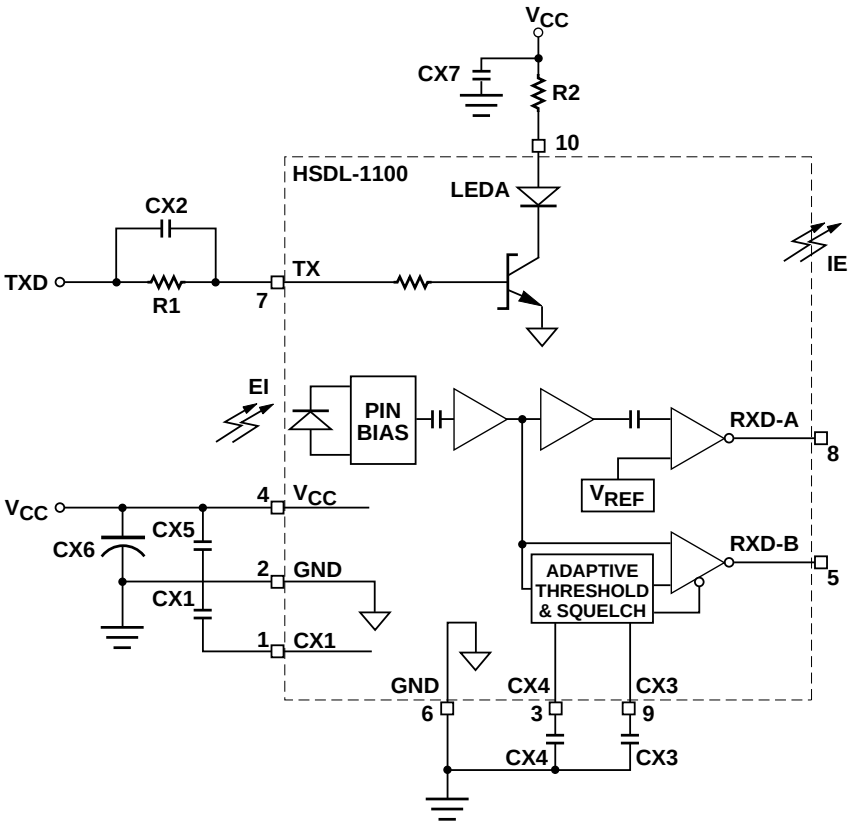


Figure 17. HSDL-1100 Circuit Diagram.

greater than 200 volts/meter for any square wave noise source, and even higher for sinusoidal noise sources. For example, a 10 volt peak-peak square wave signal source placed 5 cm from the transceiver module would produce EMI of 200 volts/meter.

Ambient Light: The HSDL-1100 receiver design allows for the ambient light levels of sunlight, fluorescent light, and incandescent light specified in the IrDA Physical Layer Specification. As with the HSDL-1001, several technologies are used in the HSDL-1100 design to reduce the effects of interfering ambient light. The package mold compound is tinted with dye to filter out visible wavelengths. The lens of the detector is designed to "see" light only within the IrDA viewing angle. The pre-amplifier for both receiver channels contains daylight cancellation circuitry to eliminate the ambient light portion of incoming IR signals.

For more information on the HSDL-1100, please refer to the Application Note, "General Application Guide for the HSDL-1100 4 Mb/s Infrared Transceiver." See also the Application Note, "Report on HSDL-1100 Interoperability with 4 Mb/s Infrared Controllers."

Endecs (Encoder/ Decoders)

The HSDL-7000 and HSDL-7001 are endec chips that perform the IrDA 3/16 Encode/Decode function for data rates up to 115.2 Kb/s, as described in the section on the IrDA Physical Layer (page 2). These devices function as the interface between a standard UART and the IR transceiver.

HSDL-7000

The HSDL-7000 performs the IrDA 3/16 Encode/ Decode function used to both encode and decode the electrical pulses for the IR transceiver. It is the interface chip between the IR transceiver and a UART. The endec requires a BAUDOUT signal which is 16x the selected baudrate. This is either supplied by the standard UART or by some external means. The HSDL-7000 is packaged in a 8 pin SOIC package. The HSDL-7000 interfaces directly to the HSDL-1001, with no external components.

HSDL-7001

Like the HSDL-7000, the HSDL-7001 performs the IrDA 3/16 Encode/ Decode function used to both encode and decode the electrical pulses for the IR transceiver. The HSDL-7001 is designed with an internal programmable oscillator for applications where the 16x clock from the serial data source may not available. This oscillator requires only an external crystal, and uses three data inputs to program the clock. These inputs may be sigals lile RTS and DTR signals from the serial port which would otherwise be unused. If a BAUDOUT signal is available, it may be used instead of the internally generated clock. For transmission, this endec adds the versatility of a 1.6 µs pulse operation. This allows baudrates lower than 115.2 Kb/s to use 1.6 µs pulses for lower power consumption. The HSDL-7001 operates on a supply voltage range from 2.7 V to 5.5 V, and is packaged in a 16 pin SOIC package. The HSDL-7001 interfaces directly to the HSDL-1001, with no external components.

Endec Netlists

For system designers who prefer to embed IrDA communications within an ASIC, Hewlett-Packard will provide the Netlist for the HSDL-7000 at no charge. The HSDL-7000 is about 200 gates of logic, and the HSDL-7001 is about 1000 gates. This may be useful for system designers who do not require the functionality of a full I/O chip, and who do not wish to use a discrete UART. With the IR modulation/ demodulation function incorporated into the system ASIC, it can connect directly to the IR transceiver module. Please refer to the Application Note, "IrDA Physical Layer Implementation for Hewlett-Packard's Infrared Products" for further information.

Discrete Emitters and Detectors

Hewlett-Packard makes a number of discrete IR emitters and detectors for supplementing an IrDA link or for proprietary applications. In many cases, it may be desirable for a designer to utilize the basic IrDA framework but make minor modifications for a particular requirement. For example, a particular application may require data transfer over distances greater than 1 meter, or size and power constraints may dictate a low power, short distance, subminature solution.

For long distances applications, Hewlett-Packard manufactures IR emitters in a variety of package styles. These emitters may be used to supplement the IR output of the transceiver modules by connecting the emitters in series, or by using the HSDL-1001's capability to drive an external emitter. For more details on extended distance applications, please see the section on Extended Distance (page 20).

For low power, space constrained applications where a full meter distance is not required, Hewlett-Packard manufactures IR emitters and detectors in subminature packages. These products enable development of "IrDA compatible" short distance links. A number of support circuits are available, or the analog functions can be incorporated into the systems ASIC.

A complete description of these products is available from the HP fax back service, or the HP web site, www.hp.com/go/ir.

Evaluation and Developer Kits

Evaluation Kits

Evaluation kits that demonstrate link functionality and proper board layout are available for the 115.2 Kb/s and 4 Mb/s products. The HSDL-8000 includes evaluation boards with the HSDL-1001 for 115.2 Kb/s links, and the HSDL-8010 includes evaluation boards with the HSDL-1100 for 4 Mb/s links. Each kit contains 2 boards, supplemental discrete LEDs (HSDL-8000 only) and documentation. These kits can greatly reduce the development time of the physical layer by providing known good transmitters and receivers, so a link can be up and running quickly. These boards exhibit the recommended design and layout techniques described in this Guide and can be used as a reference for a custom layout. The boards are ready to connect to an I/O device. The HSDL-8000 (115.2 Kb/s) board comes with an endec for serial port applications. Discrete IR LEDs are included in these kits for extending link distance or achieving greater viewing angles for non-IrDA links.

Developer Kit

The HSDL-8001 Developer's Kit provides several tools to assist a developer in designing an IrDA port into a product. This kit includes two IrDA adapters (with external power supplies) for PC serial port use, two 115.2 Kb/s evaluation boards with endecs, supplemental discrete LED's, PC software, programming libraries, and documentation. The combination of hardware and software provided in this kit allow a developer to experiment with and display how the IrDA protocol establishes and maintains a link. By using the programming libraries included in this kit, a developer can establish a simple (non-IrDA) infrared link between a PC and the developer's serial I/O device. And, the software provides a tool to perform simple testing and debugging of the developer's implementation of the IrDA protocol.

Other Products

Please be sure to check the fax-back service or HP's World Wide Web site (http://www.hp.com/go/ir) for updates to specifications, new app notes, and for information on other products as they become available.

Design Guidelines

At this point the block diagram can be frozen. All that is left to finalize the schematic is selection of the external passive components. This section describes choosing appropriate external components, and the details of board layout and other mechanical considerations.

External Passive Components

External passive components are required, and vary with each transceiver. Below are listed the components that are required and the function of each.

HSDL-1001

Refer to the schematic, Figure 18. The following components are recommended or required:

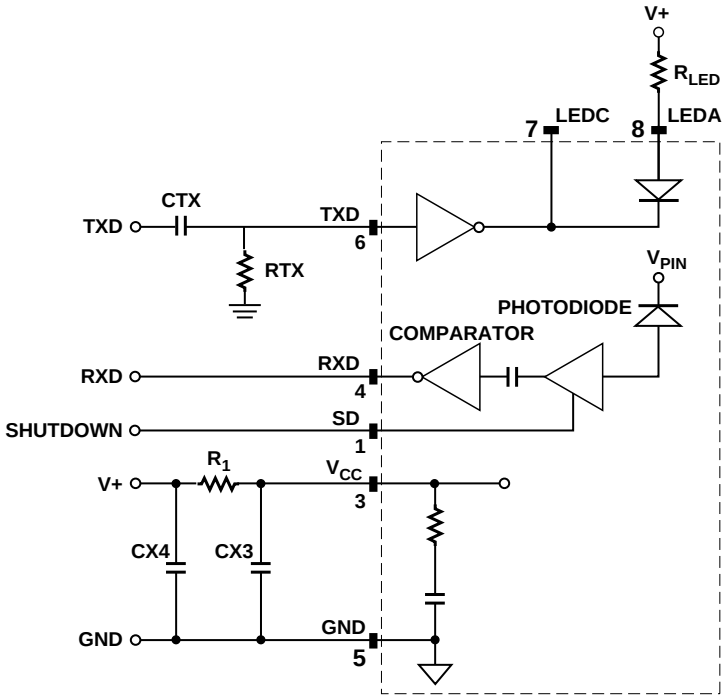


Figure 18. HSDL-1001 Schematic Diagram.

Component	Description	Recommendation
CX3	Vcc to GND bypass. Must be within 0.5 cm of pins 3 and 5.	0.1 μF, ±20% X7R ceramic. Physically small to be as close to module as possible.
CX4	Vcc to GND bypass capacitor.	4.7 μF, ±20% tantalum. Can be larger value to improve noise immunity.
RLED	LED Current Limiting resistor. Choose. RLED to guarantee the minimum required ILED (240 mA to guarantee 40 mW/sr). (See data sheet)	0.8 to 10 Ω, 0.5 watt. Value dependent upon Vcc. Calculated by subtracting the maximum LED anode voltage (i.e. 2.5 V at 240 mA, from the data sheet) from Vcc, and dividing by the required ILED current.
R1	Power Supply noise filter resistor optional, required only with noisy supplies.	50 to 200 Ω, 0.125 watt. The higher the value, the lower the minimum filter frequency, $f_c = 1/(2\pi R1*CX3)$.
RTX	AC Couple TXD. See Note.	2 KΩ
CTX	AC Couple TXD. See Note.	Nominally 0.1 μF in order to minimize pulse width distortion.

Note: RTX and CTX are only necessary in applications where the Txd pulse can exceed 90 μs, such as interfacing to the National Semiconductor PC78334.

HSDL-1100
Refer to the schematic, Figure 19. Please see also the HSDL-1100 App Note. The following components are required:

Component	Description	Recommendation
R1	TXD input resistor fro transmitter peaking.	550 Ω ±5%, 0.125 watt
R2	LED bias resistor which sets LED current pulse amplitude.	4.7 Ω ±5%, 0.5 watt
R3	Power supply noise filter resistor. The higher the value, the lower the minimum filter frequency. $f_c = 1/(2\pi R3*CX5)$.	10 – 50 Ω ±5%, 0.125 watt
CX1	PIN bypass capacitor to reduce noise at the PIN detector.	0.47 µF, ±10%, X7R ceramic, <0.5 cm from pin 1
CX2	TXD input capacitor for transmitter peaking.	220 pF, ±10%, X7R ceramic
CX3	Adaptive threshold capacitor.	4700 pF, ±10%, X7R ceramic
CX4	Adaptive threshold averaging capacitor.	0.010 µF, ±10%, X7R ceramic
CX5	Vcc to Gnd bypass capacitor. Should be within 0.5 cm of module pins 2, 4.	0.47 µF, ±20%, X7R ceramic, <0.5 cm lead length, within 0.5 cm from pins 2, 4.
CX6	Vcc to Gnd bypass capacitor.	6.8 µF, Tantalum. Can be larger to improve noise immunity.
CX7	LED Supply bypass capacitor. Only necessary where transmitter switching causes more than 50 mV ripple on Vcc.	0.47 µF, ±20%, X7R ceramic

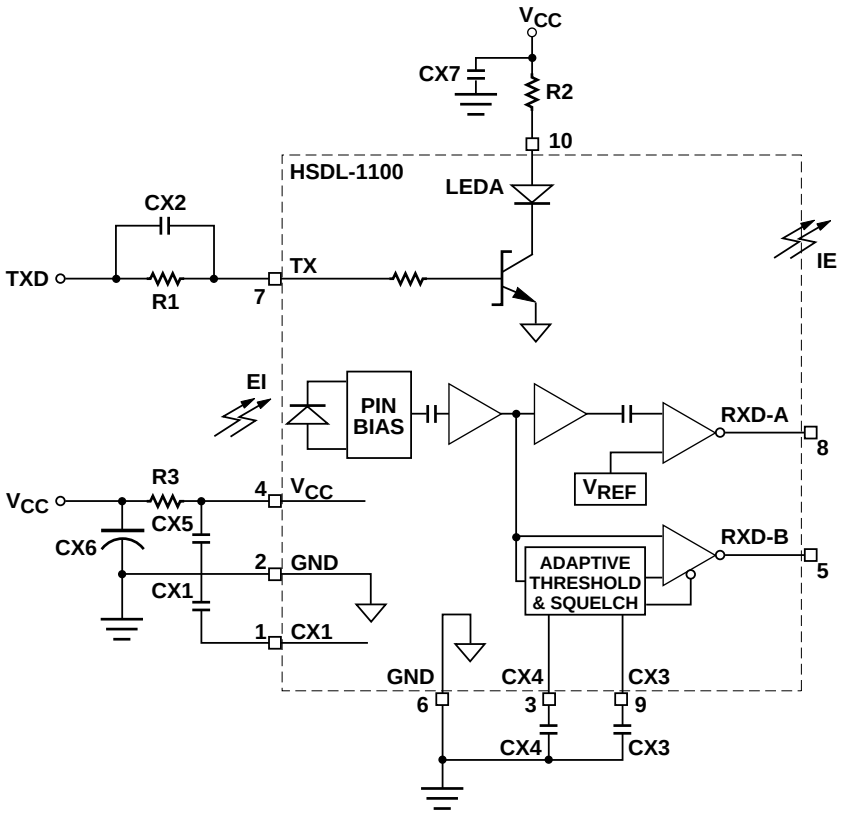


Figure 19. HSDL-1100 Schematic Diagram and Pinout Description.

Board Layout Guidelines

Lead Bend Options and Pad Layout

A number of lead bend configurations are available for each product. This variety allows the optical axis to be perpendicular to the board, parallel to the board, or, for the HSDL-1001, even straddle the middle of the board. Figure 20 shows the lead bends that are available and the corresponding option codes.

Please refer to the individual product data sheets for PC board pad layout information.

Electrical

All IR transceivers contain high gain, high bandwidth circuits. Design and board layout when using such components requires that special attention be paid to noise sources. As with many analog components, efforts should be made to separate the IR transceiver from sources of electromagnetic noise (EMI), and to minimize power supply and ground line noise. The effects of EMI and power supply noise can potentially reduce the sensitivity of the receiver, resulting in reduced link distance. EMI can also generate spurious signals on the receiver output RXD when no IR signal is being received. Evaluation kits which demonstrate the recommended board layout for each transceiver model are available, and can be obtained from your local Hewlett-Packard Component Sales Representative. These kits are further described on page 13.

EMI Immunity

EMI is radiated by switched mode power supplies, dc/dc converters, external monitor I/O ports, power ports, or clock generators. The voltage of the EMI source and the distance from the source determine the strength of the EMI field at any given point. EMI field strength is measured in Volts/meter. A 200 volt source placed 1 meter from a detector represents a field strength of 200 v/m. Similarly, 10 volt source at a distance of 5 cm also represents a field strength of 200 v/m.

An IrDA receiver's EMI Immunity is the maximum EMI field strength that the receiver can tolerate while maintaining a bit error rate (BER) < 10^{-8}. The EMI immunity of HP transceivers is typically greater than 200 v/m. Thus, the distance of the EMI source to the transceiver must be increased so that the EMI field strength is less than 200 v/m at the transceiver module.

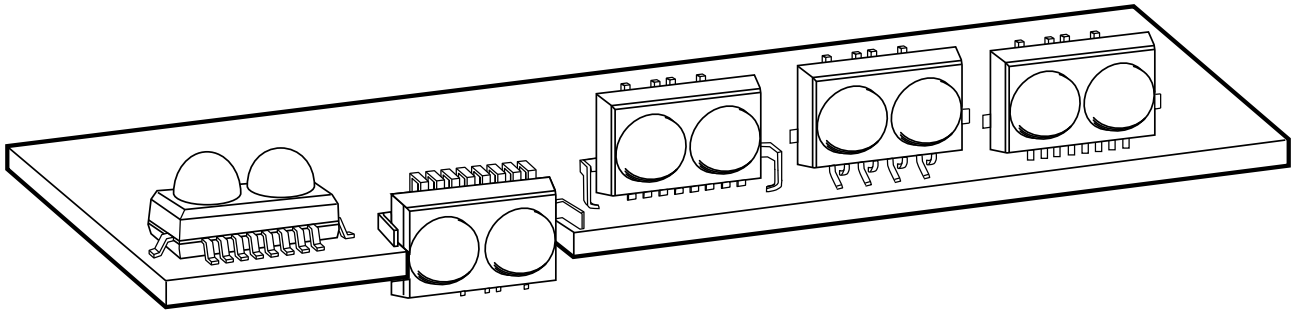


Figure 20a. HSDL-1001 Lead Bend Options.

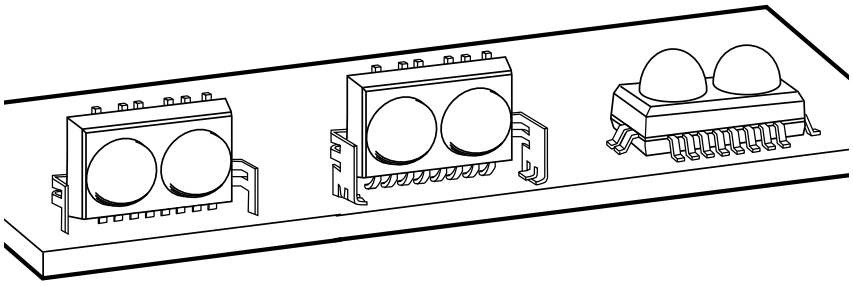


Figure 20b. HSDL-1100 Lead Bend Options.

In some cases, it may be impossible to minimize the electric field strength at the transceiver module location, such as when close to cold cathode fluorescent drivers or displays. In these cases it may be required to shield the transceiver. Hewlett-Packard has designed a number of shields for various applications Please see the Application Note, "Infrared Transceiver PC Board Layout for Noise Immunity" for further information.

Power Supply Rejection (PSR)
Power supply noise can be coupled into the receiver through Vcc or ground lines. Power supply ripple is a common example of power supply noise. PSR (Power Supply Rejection) refers to the transceiverís ability to tolerate power supply noise, while maintaining error free operation. Proper PCB layout techniques and external component placement can ensure successful operation with power supply noise present on Vcc or ground.

Board Layout Guidelines
The following recommendations for PCB layout should provide sufficient EMI immunity and power supply rejection for error free IR link operation. Please see also the Application Note, "General Application Guide for the HSDL-1100 4 Mb/s Infrared Transceiver."

1. Board Topology: A multi-layer PC board is recommended so that a sufficient ground plane can be properly placed. Use one layer underneath and near the transceiver module as Vcc, and sandwich that layer between ground connected board layers. For example in a 4 layer board, layer 1 (top) contains signal traces, layer 2 contains ground underneath the module and surrounding areas, layer 3 contains Vcc, layer 4 (bottom) contains traces and ground metal.

The area underneath the module, and 3 cm in any direction around the module is defined as the critical ground plane zone. The board's ground plane should be maximized in the critical ground plane zone. Any unused board space in the critical ground plane zone should be filled with ground metal. Unused board space is defined as board space not used for other connections or traces.

The side "buttress" leads on the HSDL-1001 are connected to internal nodes of the transceiver, and should be left electrically isolated on the PC board and should not be connected to the ground plane. The side leads on the HSDL-1100 serve as device pins. One of the side pins (pin 10) on the HSDL-1100 is also used for LED heat dissipation and needs to connect to an enlarged area of PC board metal. See the discussion on Thermal Management below.

The ground plane for the transceiver should have a very low impedance path to a clean, noiseless ground node. Ground noise at the module should be less than 75 mV peak to peak. The ground plane should be separated as much as possible from the ground traces and ground planes that are used by noisy sources such as power converters and monitor ports. A "starred" ground connection, as shown in Figure 21 is preferred.

2. External Components: Vcc bypass capacitors (CX3 for the HSDL-1001, CX5 for the HSDL-1100) and the PIN bypass cap (CX1 for the HSDL-1100) should be low inductance X7R ceramic. They should be positioned as close as possible (<0.5 cm) to the Vcc and GND pins of the module, and on the same side of the board as the transceiver. The Vcc bypass caps should used in parallel with the larger value tantalum capacitors (CX4 for the HSDL-1001, CX6 for the HSDL-1100) to extend the frequency range of the bypass. The remaining components should be placed within the board area where the ground plane has been maximized. All external capacitors should be placed as close to the module as possible. The ground plane metal can be extended beyond the critical ground plane zone in order to accommodate components, or to further improve EMI immunity.

3. Vcc Supply: The least noisy power source available on the application board should be chosen for Vcc of the module. Biasing Vcc directly from a noisy switched mode power supply line

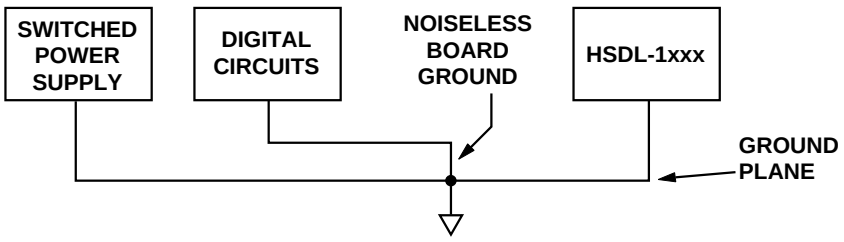


Figure 21. Starred Ground Connection.

should be avoided. The Vcc line to the transceiver module should be filtered sufficiently so that less than 75 mV of noise is present at either the Vcc or GND pins of the module. The recommended values of the Vcc bypass capacitors should provide sufficient filtering in most cases, but may be increased in value if more filtering is necessary. In some cases with the HSDL-1001, it may be necessary to provide a low value resistor (< 100 ohms) between CX3 and CX4 to form a pi filter. This configuration is the standard recommendation for the HSDL-1100.

4. Proximity to Noise Sources:
All signal or noise sources (power ports, monitor ports, clock generators, switched mode power supplies) should be placed as far away as possible so as to minimize EMI at the module. Distance to noise sources should be considered in all dimensions, including other circuit boards that may be either above or below the transceiver module, or flex circuits that may have a noise source "folded" close to the transceiver in the final assembly.

5. Thermal Management:
Because of the high power levels required to transmit at 4 Mb/s, the PC board for the HSDL-1100 should be designed to dissipate heat from the transmitter's LED. The thermal resistance of the LEDA trace on the HSDL-1100 (pin 10) should be less than 100°C/W. This will keep the LED junction temperature to less than 125°C with an LED current of 660 mA and a 25% duty cycle at 70°C ambient temperature. Such a board thermal resistance can be realized with pin 10 connected to a trace that is at least 38 mm^2, with no point narrower than 2.5 mm. For more information, please see the Application Note, "General Application Guide for the HSDL-1100 4 Mb/s Infrared Transceiver."

Troubleshooting
If the receiver is exhibiting reduced sensitivity, or the link distance is less than expected with a known good transmitter, then EMI noise or power supply noise should be suspected. The signal on RXD of the receiver should be measured with the link in an idle state (no IR transmission). If bits are observed on RXD, then noise is coupling into the receiver causing spurious bits on RXD. The receiver should then be biased from a separate clean DC supply (such as a battery). If spurious bits are still observed on RXD of the receiver, then the noise is most likely due to EMI. If RXD looks clean when biased from a separate DC supply, then the noise is most likely Vcc or Ground noise. If noise is suspected of being the problem make sure that the Board Layout Guidelines (previous section) are followed, or consult the Application Note, "Resolving IrDA Physical Layer Implementation Problems" for recommendations.

Optical Port Design

Aperture Dimensions and Shape
To ensure IrDA compliance, there are constraints on the height and width of the optical port. Minimum dimensions ensure that the IrDA cone angles are met, and maximum dimensions ensure that the effects of stray light are minimized. Figure 22 shows a

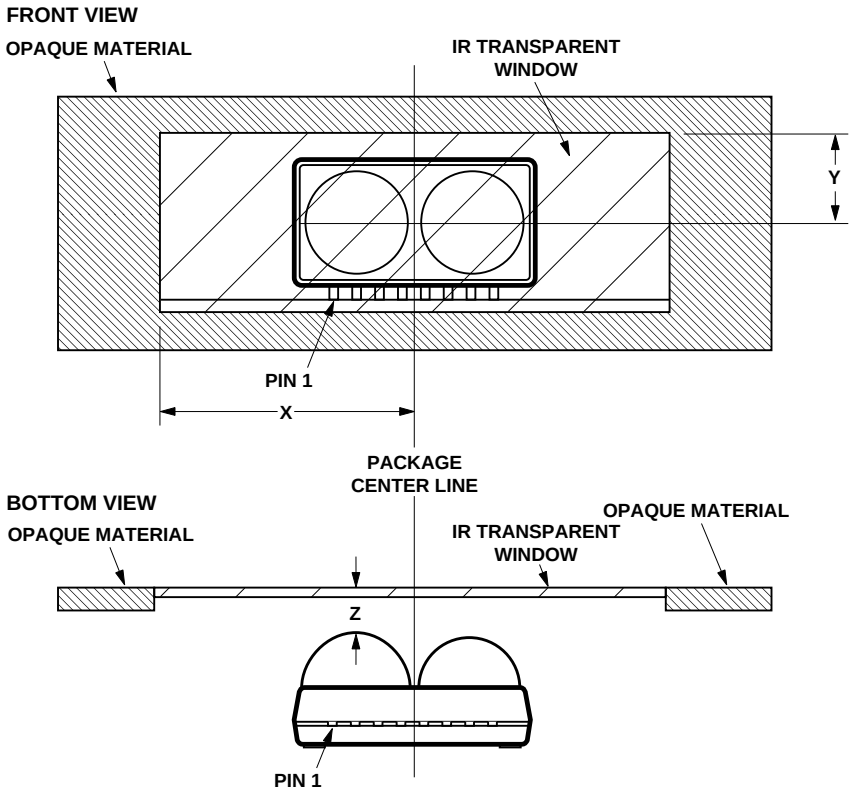


Figure 22. Position of Module with Respect to Product Case.

module positioned with respect to the front panel of a hypothetical product. Dimension 'Z' is the depth the transceiver is recessed into the case, and is defined as the distance between the apex of the receiver lens and the outside face of the front panel. Dimension 'X' is called the 'Aperture Half Width' and is defined as the distance from the middle of the module to the edge of the IR transparent window along the long dimension of the module. Dimension 'Y' is called the 'Aperture Half Height' and is defined as the distance from the middle of the module to the edge of the IR transparent window along the short dimension of the module. For a design with the module recessed a particular distance (dimension Z), the Aperture Half Width 'X' and aperture Half-Height 'Y' must be between the min and max lines in Figures 23 and 24. Designing the window within these limits will ensure IrDA radiation angle compliance. For dimensions greater than 5 mm, the following equation can also be used to calculate X and Y (units are in mm):

Xmin = 0.5774 * Z+ 7.67

Xmax = 1.732 * Z + 11.02

Ymin = 0.5774 * Z + 4.67

Ymax = 1.732 * Z + 8.02

If a cosmetic window is placed in front of the IR module, it should be flat instead of curved. A curved window will alter the radiation pattern of the LED, which may result in failing IrDA compliance.

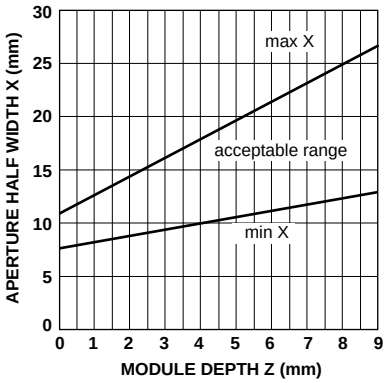


Figure 23. Aperture Half Width (X) vs Module Depth (Z).

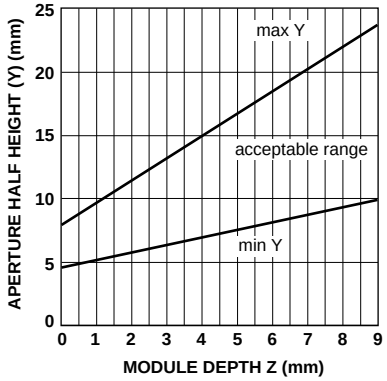


Figure 24. Aperture Half Height (Y) vs Module Depth (Z).

Window Material Selection
The HSDL-1001 data sheet specifications for Transmitter Radiant Intensity and for Receiver Input Irradiance allow for 10% IR signal loss through a cosmetic window placed in front of the IR transceiver module. The recommended plastic materials for use as a cosmetic window are available from General Electric Plastics (see References). The recommended dye is Violet #21051 (IR transmissant above 625 nm). See Table 2 for the recommended Plastic Materials.

Improved receiver performance in the presence of ambient light (sunlight, fluorescent light, incandescent light) can be attained by recessing the module into the system case by a few millimeters. The overhang of the system box will minimize the amount of direct ambient light that the receiver sees. The cosmetic window will also help reflect ambient light away from the module.

Eye Safety

Eye safety may be a consideration in some IR systems. Most implementations with Hewlett-Packard IrDA transceivers are within eye safety guidelines when used as recommended , even under single fault conditions. However, at sufficient power levels, the heating effects of IR energy can damage the retina. Further, the eye is not able to adapt to bright IR sources. The amount of heating will vary with apparent source size, distance, and duty cycle. HP optics are carefully designed to optimize eye safety.

Eye safety is a topic that is being considered by a number of international safety and regulatory agencies. For the most recent information on IR and eye safety, please consult the Application Note, "Compliance of Infrared Communication Products to IEC 825-1 and CENELEC EN60825-1."

Table 2.

Material #	Light Tranmission	Haze	Refractive Index	Thickness
Lexan 141L	88%	1%	1.586	1/25 to 1/8 inch
Lexan 920A	85%	1%	1.586	1/25 to 1/8 inch
Lexan 940A	85%	1%	1.586	1/25 to 1/8 inch

Beyond IrDA

Extending Transmission Distance

In some cases, it may be desired to increase link distance beyond the 1 meter guaranteed by IrDA. The two ways to do this are to increase transmitted light intensity, or to increase receiver sensitivity. In order to extend the link distance, both sensitivity and intensity must be increased on one end of the IR link, or either sensitivity or intensity must be increased for both ends of the IR link. If it is desired to communicate with a standard IrDA device that may have minimum transmitter intensity, the receiver sensitivity must be increased. The standard IrDA device may also have minimum receiver sensitivity, so transmitter intensity must also be increased.

Assume there are two ends of an IR link labeled A and B. If both sensitivity and intensity are increased for end A, then A's transceiver can both receive and transmit at longer distances regardless of what transceiver is at end B. If only transmission intensity is increased for end A, then the transmission intensity of end B must also be increased in order to increase link distance. Otherwise, B's transceiver could move further from A and still receive A's signal, but A could not receive B's transmitted signal. The same is true if only receiver sensitivity is increased.

A link with an HSDL-1001 at each end will transmit data from 0 cm to 1 meter over all recommended operating conditions with a bit error rate of less than 10^{-8} and still be IrDA compliant. Under typical operating conditions, the link distance can reach 2 meters.

Typical link distance can be increased if both ends of the IR link increase their transmission intensity. Radiant intensity is approximately proportional to LED forward current, and irradiance (the strength of the received IR signal) will follow the inverse square law for distances greater than a few cm. For example, four times the LED forward current will provide four times the intensity. Four times the intensity will give the same signal strength at two times the distance. If the LED current pulse amplitude of both ends of the IR link are increased from the recommended 240 mA to 500 mA, the link distance can typically reach as far as 2.8 meters at 115.2 Kb/s, and about 1.4 meters with worst case operating conditions.

The HSDL-1001 features the ability to drive an external LED for added power. Either the HSDL-4220 or the HSDL-4230 IR emitter can be connected in series or in parallel with the HSDL-1001's internal LED. (Note that the parallel connection will only work with 5v supplies.) The HSDL-4220 typically provides 190 mW/sr of intensity at a peak pulse current of 250 mA, and has a viewing angle of 30 degrees. The HSDL-4230 typically provides 375 mW/sr of intensity at a peak pulse current of 250 mA, and has a viewing angle of 17 degrees. Refer to the HSDL-4220 and HSDL-4230 datasheets for more information on these products.

For 5v systems, a parallel connection (Figure 25) may be used. The drive transistor of the HSDL-1001 has sufficient capacity to drive a second LED in parallel. The current in the external LED is limited by RLEDX. The value if RLEDX is chosen in the same manner as RLED (see the section

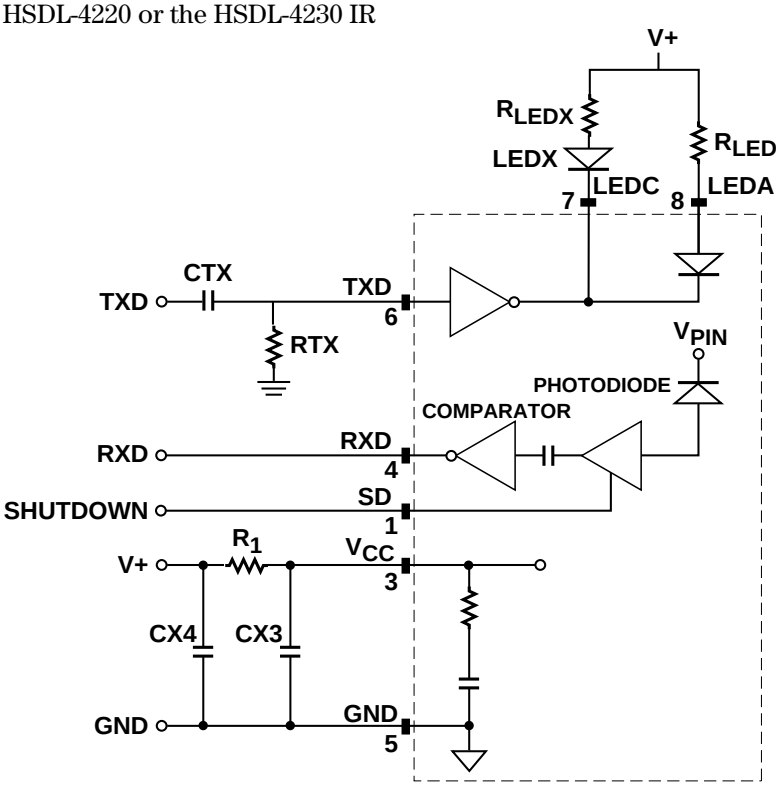


Figure 25. External Parallel LED.

on External Passive Components). This configuration has the advantage of being less sensitive to power supply variations than the series connection, because more of the supply voltage is dropped across the limiting resistors.

The series, or "stacked" connection (Figure 26) can be used with supplies greater than 5 V. This connection is preferred because it uses power that would otherwise be wasted in RLED. This configuration can be used when Vcc is high enough to allow for two forward voltage drops (2.5 V each at 240mA) and the tolerance is tight enough so that the RLED chosen for minimum Vcc does not cause excessive currents at maximum Vcc.

The combined intensity of the HSDL-1001 internal LED and the HSDL-4220 or HDSL-4230 external LED can be used to calculate the potential link distance. Link distance is proportional to the square root of the total intensity of the signal. Table 3 shows the typical link distances which can be achieved under typical operating conditions with various external LEDs driven as indicated. Worst case conditions will, of course, yield reduced guaranteed link distances. Figure 27 shows in graphical form the typical distance that can be expected as a function of transmitter intensity.

Table 3.

Transmitting Devices	LED Pulsed Drive Currents (Ipeak)	Total LED Typical Intensity On-Axis	Typical On-Axis Link Distance
HSDL-1001	250 mA	100 mW/sr	2.0 meters
HSDL-1001	500 mA	200 mW/sr	2.8 meters
HSDL-1001 and HSDL-4230	250 mA each	290 mW/sr	3.4 meters
HSDL-1001 and and HSDL-4230	500 mA each	950 mW/sr	6.1 meters
HSDL-1001 and and 4 HSDL-4230s	500 mA each	3200 mW/sr	11.3 meters

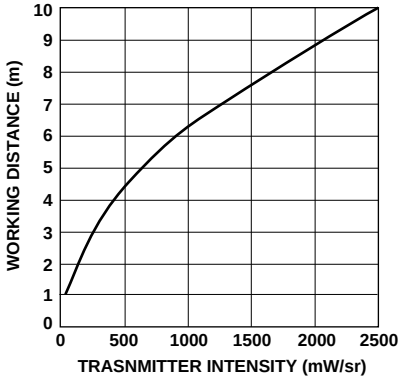


Figure 27. Typical Distance vs. Transmitter Frequency.

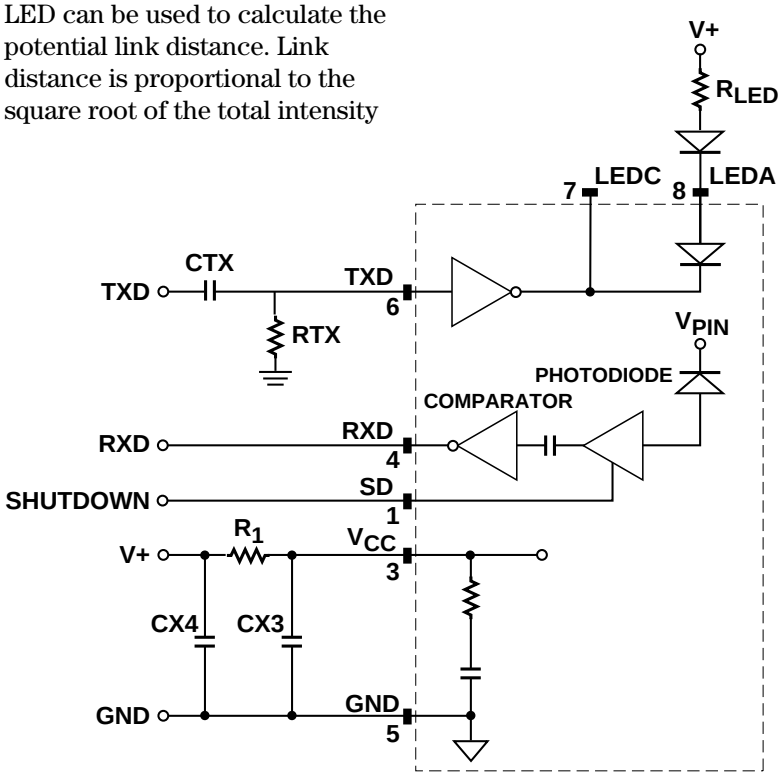


Figure 26. External Series LED.

For data rates of less than 115.2 Kb/s, transmitting signals with less than 20% duty cycle can help to increase link distance. The receiver threshold is determined by average power, so a lower duty cycle will reduce average power and thus increase the receiver's sensitivity. Also, to minimize power consumption and increase LED life, it is recommended to use the minimum pulse width allowed by IrDA, which is 1.6 µs.

ASK, DASK and TV Remote

It is possible to transmit and receive signals other than IrDA signals with Hewlett-Packard IR transceivers. For implementation details, please refer to the Application Note, "Transeiver Performance with ASK and TV Remote Signals."

Appendix A. Basic Radiometry

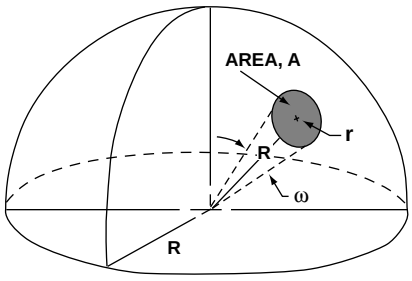
Steradian (ω)

Measurement unit of a solid angle.

A steradian is the solid angle subtended from the center of a sphere by 1/4π of the surface area of the sphere. There are 4π steradians in a full sphere.

A cone of a solid angle ω, has its apex at the center of a sphere of radius R and defines an area A on the surface of the sphere. To find a solid angle (ω), determine the surface area of the sphere included within the solid angle (A), and divide the area by the square of the radius of the sphere (R).

$\omega = A / R^2$



A solid angle of one steradian can be visualized as a cone with an apex angle of 65.6 degrees.

Radiant Intensity (Ie)

Measurement unit of emitted power per steradian (mW/sr).

Intensity is the optical power per solid angle delivered by a source. The on-axis intnesity of an LED is described by Ie.

Irradiance (E)

Measurement unit of received power per unit area (mW/cm^2).

Irradiance is the power per unit area incident on a surface. The amount of power received by a detector is described by E.

Inverse Square Law

Law that determines the amount of power incident on a surface.

If a surface is X cm from a point source, then 1 cm^2 of that surface subtends $1/X^2$ steradians (A/R^2) as seen from the point source. The amount of power falling on the 1 cm^2 surface is calculated by multiplying the intensity of the point source in mW/sr by the number of sr/cm^2. This gives the irradiance on the surface (detector).

Example:

An LED is 120 cm from a detector.

The Ie of the LED is 75 mW/sr.

The Responsivity of the detector is 6 $\mu A/mW/cm^2$.

Angle subtended from the LED to a (hypothetical) 1 cm^2 detector, in steradians, is:
$1\ cm^2/(120cm)^2 = .0000694\omega$

Irradiance on the detector =
$75\ mW/sr * .0000694\ sr/cm^2 =$
$5.21\ \mu W/cm^2$.

Photocurrent from detector =
$5.21\ \mu W/cm^2 * 6\ \mu A/mW/cm^2 =$
31.3 nA.

Viewing Angle ($2\theta_{1/2}$)

The viewing angle is described as twice the half angle. The half angle ($\theta_{1/2}$) is the angle from the normal at which either the LED brightness or the photodiode responsivity is reduced by 50%.