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APPLICATION NOTE 6.17

Definitions and Differences Between I^{2}C, ACCESS.bus and SMBus

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Overview

This document describes and explains differences between some of the most used serial communications protocols such as I^{2}C, ACCESS.bus, and SMBus. Reader must be familiar with these protocols, for more detailed specification on each protocol, refer to Supporting Documents section.

A system using a serial communications protocol passes messages to and from devices instead of tripping individual control lines. Removing the individual control lines reduces pin count.

Background

These serial communication protocols consist of a serial data line (SDA) and a serial clock line (SCL). Both lines are connected to a positive supply via a pull-up resistor, and remain HIGH when the bus is not busy. Each device is recognized by a unique address; Whether it is a micro-computer, LCD driver, memory or keyboard interface and can operate as either a transmitter or a receiver.

Every device connected to the bus must have an open-drain or an open-collector output for both the data (SDA) and the clock (SCL) lines.

Data on the bus can be transferred at up to 100Kbit/s. The number of devices connected to the bus is limited only by the maximum bus capacitance.

ACCESS.bus is a serial communication protocol allowing a computer host to communicate with external (off-board) peripherals as well as with internal (on-board) system devices. Because of the difference in the electrical requirements between devices operating externally to the system and devices operating internally within the system box, peripherals operating externally to the system box specify maximum capacitance and cable lengths.

SMBus is also a serial communication protocol allowing a computer host to communicate with internal (on-board) system devices.

The SMBus may share the same host device and physical bus as ACCESS.bus components provided that an appropriate electrical bridge is provided between the internal SMBus devices and external ACCESS.bus devices.

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Both ACCES.bus and SMBus use I²C as their backbone.

SMSC Bus Support

SMSC PART NUMBER	I2C	ACCESS.bus NOTE 1	SMBus NOTE 2
FDC37C93xFR	✓	✓	✓
FDC37C93xAPM	✓	✓	✓
FDC37C95xFR	✓	✓	✓

Note 1: ACCESS.bus can easily be interfaced to SMSC parts by allowing at least fifty microseconds between releasing bus mastership and requesting to become bus master again. This is done in software.

Note 2: SMBus logic levels are easily met using standard 5 volt components.

Bus Differences

I^2C Vs ACCESS.bus

The major differences between I^2C and ACCESS.bus fall into several categories including electrical, timing, protocol, and physical characteristics.

I^2C Vs Off-board ACCESS.bus

Elecrical

1. The VCC and GND are supplied by the host in addition to the SDA and SCL. The I²C-bus has only SDA and SCL lines.
2. IOL = 6mA for the Off-board ACCESS.bus, vs. IOL = 3mA for the I²C-bus. The pull-up resistors and the serial resistors for Off-board ACCESS.bus operation were decreased to allow IOL = 6mA.
3. The maximum capacitance per line was increased from 400pF for the I²C-bus to 1000pF on the Off-board ACCESS.bus.

Protocol

1. ACCESS.bus device must allow at least fifty microseconds (50 microseconds) between releasing bus mastership at the end of a message and requesting to become bus master again. This is to give other devices a chance to access the bus without arbitration, I²C does not specify any delay for releasing bus mastership at the end of a message.
2. ACCESS.bus interfaces shall not hold SCL low for more than two milliseconds (2ms). A watchdog timer or other provision shall be implemented by each device to assure it releases SCL before the two millisecond (2ms) limit is reached. I²C specification does not specify a time limit on how long it can hold SCL low.
3. For ACCESS.bus, the master device always transmits data to a slave. In I²C-bus protocol the master can also read from the slave.
4. Every device connected to the Off-board ACCESS.bus must be capable of being a bus master and a bus slave.

Physical

1. The Off-board ACCESS.bus specifies a connector and a cable. I²C-bus does not.
2. The Off-board ACCESS.bus maximum cable length without a repeater is 10 meters. The I²C-bus does not define a maximum cable length.

I^2C Vs On-board ACCESS.bus

Electrical

1. IOL = 350µA for the On-board ACCESS.bus, vs. IOL = 3mA for the I²C-bus. It is recommended that the pull-up resistors be replaced by current sources.
2. The maximum capacitance per line of 400pF for the I²C-bus was replaced with required rise and fall times for On-board ACCESS.bus devices.

Protocol

1. ACCESS.bus device must allow at least fifty microseconds (50 microseconds) between releasing bus mastership at the end of a message and requesting to become bus master again. This is to give other devices a chance to access the bus without arbitration, I²C does not specify any delay for releasing bus mastership at the end of a message.
2. ACCESS.bus interfaces shall not hold SCL low for more than two milliseconds (2ms). A watchdog timer or other provision shall be implemented by each device to assure it releases SCL before the two millisecond (2ms) limit is reached. I²C specification does not specify a time limit on how long it can hold SCL low.

SMBus Vs I²C

The major differences between SMBus and I^2C fall into several categories including electrical, timing, and protocol.

Electrical

1. SMBus is based on fixed voltage levels, the I²C levels are scaleable. However, the SMBus logic levels are easily met using standard 5 volt components.
    a) The I²C bus references its electrical characteristics to Vdd. Components attached to SMBus may operate at different voltages. Therefore the SMBus cannot assume that all devices will share a common Vdd, hence fixed voltage logic levels.
2. SMBus specifies a minimum operational clock speed (10 KHz), I²C minimum operational clock speed (0 KHz).

Timing

1. SMBus device must allow at least fifty microseconds (50 microseconds) between releasing bus mastership at the end of a message and requesting to become bus master again. This is to give other devices a chance to access the bus without arbitration, I²C does not specify any delay for releasing bus mastership at the end of a message.
2. SMBus interfaces shall not hold SCL low for more than two milliseconds (2ms). A watchdog timer or other provision shall be implemented by each device to assure it releases SCL before the two millisecond (2ms) limit is reached. I²C does not specify specification has no time limit on ho long it can hold SCL low.
3. SMBus allows a master device to stretch the cumulative clock (low) time, in any single byte, up to Tlow:mext. This allows, for example, a keyboard controller-based SMBus emulation sufficient time to service keyboard interrupts while hosting the SMBus.
4. SMBus allows a slave device to stretch the cumulative clock (low) time, in a single message, up to Tlow:sext. This allows, for example, a low-power microprocessor-based slave device, such as a Smart Battery, sufficient time to “wake-up” and/or “marshal data.”

Protocol

A message destined for the host could appear from an unknown device in an unknown format. To prevent possible confusion on the host's part, only one method of communication is allowed, a modified Write Word. The standard Write Word protocol is modified by replacing the command code with the calling device's address. This protocol is used when an SMBus device becomes a **master** to communicate with the SMBus host acting as a **slave**.

SMBus Vs ACCESS.bus

The major differences between SMBus and I^2C fall into several categories including electrical, timing, protocol, and physical characteristics.

Electrical

1. SMBus has fixed voltage levels, ACCESS.bus uses .3 and .7 Vcc (presently defined at 5 volts) for logic levels.
2. SMBus does not specify a maximum bus capacitance.
3. SMBus specifies a maximum sink current pull-up (350 µa), which is considerably less than the 6 ma specified by ACCESS.bus.
4. SMBus specifies a maximum Vol (0.4 volts) less than the 0.6 volts specified by ACCESS.bus.

Timing

SMBus requires SMBus devices to respond directly as opposed to ACCESS.bus that requires a device to respond independently to a request within 40 ms. All SMBus devices are required to reset themselves in such a manner as to return the SMBus to an idle state whenever any SMBus device does not respond within $T_{timeout}$ ms.

Protocol

1. SMBus specifies fixed addresses for SMBus devices as opposed to the assignable addressing scheme specified by ACCESS.bus. However, there is a reserved SMBus address which is intended for use by future SMBus devices that may offer a limited form of assignable addressing.
2. SMBus uses both the read and write modes of I^2C. ACCESS.bus uses only the write mode.

Physical

SMBus does not specify a connector.

Supporting Documents

This specification assumes that the reader is familiar with or has access to the following documents:

1. *The I^2C-bus and how to use it*, Philips Semiconductors document #98-8080-575-01.
2. *ACCESS.bus Specifications -- Version 3.0.*
3. *The System Management Bus Specification -- Version 1.0.*