Host Signal Processing:
A Strategic Technology For Today's Computer Designers

A Brief Introduction To HSP

Designing today's personal computer systems represents an ever-more difficult challenge for the engineer. In addition to providing higher levels of performance with each new model, there is constant pressure to add new features without an appreciable rise in cost. Rather than follow the tried-and-true approach of shoe-horning ever-increasing quantities of logic gates into their products, more and more designers are turning to Host Signal Processing (HSP) technology to help them meet the demands of this rapidly evolving market.

MIPs vs. Chips

Put simply, HSP is a software-based technology that employs a portion of the unused instruction cycles (MIPs) in a host computer's CPU chip's to perform signal processing and other functions that are normally handled by a separate Digital Signal Processing (DSP) or controller chip. This has been made practical by the rapid evolution of the microcomputer.

As we shall see later, the abundance of processing power available in the recent generations of processors allows them to do significant amounts of real-time signal processing concurrently with their traditional tasks of supporting the host's operating system and resident applications. This can allow designers to eliminate everything but the small amount of electronics required to digitize an incoming signal and convert it back to analog on the way out. Using HSP-based designs enables significant savings in a product's bill of materials (BOM), assembly costs, and PC board space.

In order to use the host's computing resources without severely impacting its normal operations, an efficient interface with the operating system must be established. Within the Windows environment, a combination of hardware and software techniques are used to assure that the CPU's time is divided fairly between the HSP application and the tasks it was originally intended to perform. Often, an HSP application also uses a portion of a host's memory as a buffer and for interim storage of data while it is being processed. Surprisingly, using the host's RAM in this manner often actually improves an application's performance as well as further reducing the cost of implementing an HSP function.

HSP Applications Include "Soft Modems"

There are a number of areas where HSP is being used to reduce component counts and increase the feature sets in personal computer systems. As an example, there are several nearly-all-software realizations of the AC97 audio codec today which successfully replace an equivalent silicon solution. For computer-telephony or voice-over-Internet, speech compression software has been developed to run concurrently with most popular browsers.

One of the most interesting of the current HSP applications is the telephone data modem. Once a fairly straightforward device, the recent generations of modems have employed increasingly sophisticated modulation techniques to squeeze larger amounts of data down fixed-bandwidth telephone connections.

The most recently approved modem specification (ITU V.34) defines a 1000+ point quadrature/amplitude modulation (QAM) trellis coding scheme that can support data rates of up to 33 kbits/s. A new generation of modems using pulse-code modulation (PCM) has recently entered the market and may be able to achieve speeds of up to 56-kbit/s under certain conditions. As we shall see, both of these modem technologies are excellent candidates for implementation using HSP.

Technical and Market Forces Driving The Move To HSP Modems

Designers have long ago abandoned attempting to employ analog modulation techniques to create these complex signals, and turned to digital signal processing. With the arrival of relatively inexpensive single-chip DSPs in the late eighties, the price of high-speed modems fell from several thousands to a few hundreds of dollars.

Recently, the growing number of home offices and the explosive popularity of the Internet has has placed extraordinary price pressure on modem manufacturers and their chip vendors. With the modem now a "must-have" accessory for even the most modest home computing system, the

demand has nearly reduced modems to commodity status. Manufacturers are forced to increasingly employ higher levels of integration to shave even a few cents off a design.

Host signal processing technology is able to deliver a quantum leap in cost savings for modems. By using the system CPU to perform all the audio signal processing and protocol controller functions, a cost savings of half or more of the price of a silicon-based modem the can be realized. Several modem vendors are already realizing these savings with HSP modems on ISA-Bus and PCMCIA cards, while plans to offer PCI and USB-based HSP modems are already under way.

HSP For Motherboard-Based Telecommunications Functions

Even more savings can result if the modem is placed on the PC's motherboard, eliminating the cost of a separate PCB, its associated connectors, and other components. Much like the successful migration of Ethernet functions to the motherboard, manufacturers are beginning to realize that on-board modems are attractive both from a cost savings and because it frees up a precious bus slot for use in other applications.

Until now however, buying a computer with an integrated modem was a questionable choice, since the arrival of newer technologies and features could rapidly make it obsolete with no upgrade path possible. HSP modems however, are inherently software-upgradable, thereby eliminating the risk of obsolescence. HSP make it practical to move telecommunications functions onto the motherboard by giving users the ability to easily upgrade their modems with performance enhancements and new features as they become available.

Mobile computers add yet another set of demands on modem designers. The limited case volumes and battery capacities of laptops, palmtops, and wearable computers place both space and power at a premium.

There is great interest in HSP for portable systems because they eliminate the modem's relatively power-hungry DSP and replace it with the existing host CPU which is already drawing its share of battery current. A typical HSP-based modem such as the PCT388 series from PCTel consumes 200 mW @ 5v, compared to 500 mW for an equivalent DSP-based solution.

In PCMCIA applications, the software modem's low parts count makes integrating it into the PC card's compact form factor a much easier task, a feature that has already made it popular with several PC accessory manufacturers. Plans are in the works by at least XXX laptop producers to include it on the motherboard of their next-generation products, freeing up the PCMCIA slot for other duties.

HSP-based communications will also play an important role in the palmtop and sub-notebook arena. One of the most important functions for a PDA to perform is to keep its mobile owner in touch with e-mail, faxes, pagers, and other communication services normally associated with the office environment. As PDA's begin to find widespread use, they will begin to look less like computers and more like "communicators," extending people's access to their mission-critical information sources. HSP can be a valuable tool in meeting the power and space challenges involved with designing these communications-oriented PDAs.

Future-Proofing Products With HSP

As mentioned earlier, a software-based solution makes it easy for products to track late-breaking developments in telecommunications standards. One important example is the recently approved ITU V.70 standard for implementing voice/data (SVD) services over modems. Video conferencing technologies to support the V.80, H320, and H.324 protocols can also be realized using HSP.

Tracking the rapidly evolving standards for the recently introduced 56-kbit/s, PCM-based modems is a task that is well-suited for HSP technology. At the present time, there are two major industry alliances (Lucent/Rockwell vs. U.S.-Robotics/Texas Instruments) competing to have their version of the 56-kbit technology sanctioned as a standard for the U.S. by the T1E1 committee, and for the world by the ITU. While the U.S. standard should be finalized by the end of 1997, and refined for global applications towards the end of 1998, it would not be inconceivable for this kind of political maneuvering to significantly delay the final roll-out of PCM modem standards.

During this time, manufacturers will have to offer software-upgradable modems or risk having their products become obsolete within less than a year. Whereas conventional modems must bear the additional expense of adding flash memory to permit field upgrades, HSP modems require no new components to be able to upgrade from a disk, bulletin board, or download up-to-date software from the manufacturer's Web site.

Software-Based Features For Product Differentiation

A software-intensive solution also helps address the proliferation of "value-added" features, such as full-duplex speakerphones, fax capabilities, and answering machines, that are becoming common in modems. Keeping these features RAM-resident means that manufacturing lines and inventories do not have to be disrupted each time a performance upgrade or new feature is added to the product.

Concurrent Data/Signal Processing Leverages The Host CPU's Value

It has always been possible to perform limited amounts of functions typically associated with DSPs (multiply-accumulates, indexed memory operations, and other array-oriented processing functions) on standard complex instruction set (CISC) processors. Unfortunately, the earlier x86-class processors already had their hands full supporting the demands of the operating system, I/O drivers, and applications that formed the core of a PC's normal operations. The problem is compounded because it typically takes a CISC machine 50-100% more instructions and clock cycles to accomplish the multiply/accumulate operations that are hardwired into a DSPs' instruction set. For these reasons, most designers have used dedicated DSPs to perform the speech processing and modem functions in their personal computers.

This has changed recently as Intel, Motorola, DEC, and other CPU merchants have ridden the steep growth curve postulated by Moore's law for the past decade. While the cost of the processors themselves has held relatively constant, the cost of each MIP they deliver has been declining

rapidly. Thanks to investments of billions of dollars in advanced CPU design and semiconductor fabrication technologies, the vendors have consistently managed to double the amount of computing power that can be packed into the same piece of semiconductor about every 18 months. This increase has been so rapid that it has, in many cases, managed to outpace the considerable demands for more MIPs placed upon them by increasingly complex operating systems and applications.

With the introduction of Pentium-class machines, the fraction of a CPU's computing capacity required to implement a given function has begun to cost much less than the price of the LSI chips required to do the same thing. This trend is being further encouraged by the processor manufacturer, Intel. Its new CPUs with the MMX™ architecture contain an extended instruction set which allows them to perform DSP-like functions in a fraction of the machine cycles required for a conventional CISC machine.

The final factor in the equation is Microsoft's Windows '95, the de facto standard operating system for today's consumer-grade computers. While they present problems in some other areas, the '95 and NT operating systems do offer the advantage of support for support multi-threaded, multi-tasking operations. This makes the HSP modem's CPU-intensive real-time line coding and equalization functions much easier to implement.

Implementing HSP-Based Designs

Hardware/Software Partitioning

In order to realize the most cost savings, an HSP modem must replace as much of the original hardware as possible. Most modems on the market today will employ anywhere between four and six major ICs in their design (See Fig. 3). This typically includes a telephone line codec, a data pump (usually a DSP), a microcontroller, and a speaker driver, plus the associated RAM and EPROM. In the PCTel realization of a software modem, the count is reduced to one analog IC and one relatively small digital chip (See Fig. 3 again). The analog chip contains the only portion of the modem's original hardware that remains - the telephone line codec and line isolation circuitry. The digital chip is an ASIC which contains a small, intelligent data buffer and some sophisticated logic that performs interrupt generation and efficient, well-timed DMA block data transfers with the host. Also included is the circuitry which interfaces the modem directly to the host's ISA or PCI bus.

Host/Application Partitioning

Ideally, an HSP application should be transparent to the host system, functioning as if the traditional hardware implementation were still in place. This is accomplished by using Window's standard application programming interfaces (APIs). The OPEN_COM, WRITE_COM, and READ_COM APIs can be used to invoke all HSP functions and pass data to and from the operating system. To make the HSP modem compatible with the majority of communications software packages, it's host interface section has been designed to emulate the standard "AT" modem command set. By mapping the modem's hardware so it uses the IRQ 3 and 4 slots, its simulation of its silicon equivalent is complete.

Multi-Media Applications

On these faster machines, it becomes feasible to run other applications concurrently, or to add multimedia extensions to the software modem, or both. This means that it is feasible to implement an echo-canceling, full-duplex speakerphone, a digital simultaneous voice/data (DSVD) function, or even a significant portion of a videoconferencing system in software, provided there is a sufficiently powerful processor available. From the requirements tables below, it appears that the processing requirements for multimedia are significant, but not beyond the reach of today's computers.

PROCESSING REQUIREMENTS FOR A DSVD MODEM

Function	Pentium MIPs Required
V.34 Modem	60
G.729 Voice Compression	30
Echo-Canceling Full-Duplex Speakerphone (Optional)	30
Total MIPs Required	90-to-120

PROCESSING REQUIREMENTS FOR A V.80 VIDEO MODEM

Function	Pentium MIPs Required
V.34 Modem	60

G.723 Voice Compression	30
H.261 Video Compression	60
Total MIPs Required	150

Emulating DSP Functions On CISC Architectures

A CISC processor such as the Pentium is much like a Swiss Army knife, a device with lots of functions but not optimized for any single one. Their native instruction sets can make program branches on complex logical or status conditions, they can perform many kinds of memory addressing, and a wide variety of mathematical and logical operations.

DSPs on the other hand, have a very limited number of instructions which have been optimized to be performed in the shortest possible amount of time. Their ability to perform extremely fast multiply/accumulate operations and single-instruction indexed memory operations enables DSPs to emulate multi-tap digital filters and other complex shaping functions.

These structural differences present a problem for the software modem designer. Pentium-class processors, for example, have been optimized to perform logical operations very quickly, at the expense of the speed of executing arithmetic instructions. These are the very ones required for DSP emulation. It is possible however, with careful attention to code optimization, for very fast CISC machines to employ subroutines that emulate DSP functions. Since they are not as efficient in this mode, it is extremely important to identify the most-used operations and make sure they are done using the least possible amount of machine cycles.

Making Best Use Of The MMX Architecture

Beginning this year, Pentium processors are available with an extended instruction set that will help them accelerate multimedia applications. These Multi-Media extensions (MMX) are DSP-like functions such as 64-bit data operations and indexed memory instructions that reduce the number of machine cycles required to perform graphics vector calculations, audio filtering and compression, and other highly iterative mathematical operations.

From initial studies, an MMX-enhanced processor appears to enjoy roughly a 20% performance advantage over a standard processor while running HSP modem software. This allows a 150-MHz MMX/Pentium chip to deliver the same performance as its 180-MHz non-MMX counterpart.

Coping With Win'95 And Other "Non-Real-Time" Environments

When implementing a software modem in a Windows environment, one must be aware that its multi-tasking features don't necessarily mean it can be trusted with real-time tasks. The problem is that Windows is not a real-time operating system and is designed to take care of itself first. The operating system can become unavailable for periods of up to 60 msec. Unless some sort of compensation is made for these periods, the host can miss critical data transfers from the modem, causing "holes" in incoming or outgoing bit streams to occur.

To cope with this uncertain environment, the digital interface chip controls the timing of the data transfers, creating "time slots" during which it grabs the host processor's attention for moving and

processing modem-related data. Its on-chip buffer accumulated the codec data into conveniently-sized blocks and also keeps the data from getting lost when the host processor is momentarily unavailable. To avoid excessive latency within the modem, the buffer should not be too large, typically well under 1 kbyte. Information from the buffer is transferred via DMA to and from the host memory in somewhat smaller blocks

During each time slot, part of the input buffer's contents are transferred to and from host memory. In the event that the host is unavailable, buffer can tolerate missing several time slots before actually losing incoming or outgoing data. As soon as the next time slot rolls around, the interface chip and host software perform a recovery procedure if data is once again available. Should the processor remain unavailable past the buffer's capacity, the interface circuit can postpone disaster for an additional few milliseconds by sending "dummy" information blocks.

PDAs, Palmtops And Other Imlimentations / Applications

An HSP modem's power and space savings makes it very attractive for extremely compact, low-power PDAs, palmtop computers, and personal communicators. Unlike their laptop cousins, these ultra-compact devices do not usually employ x86 processors. Instead, they often use low-power RISC machines, such as the ARM, StrongARM, the NEC MIPS 3000 and the family of Hitachi CPUs. While not as fast as a typical Pentium, most RISC processors' instruction sets have math functions which can do a surprisingly good job of efficiently mimicking DSP tasks. Additionally, the compact operating systems used by these machines often have provisions for supporting real-time operations like HSP.

Not surprisingly, HSP modems have enjoyed rapid acceptance in the sub-laptop market. It can already be found in the new Philips Velo, and will soon be availible in several other highly popular units. While the current generation of processors can only run HSP software fast enough to support data rates of 14.4 to 19.2-kbits/s, improvements in clock speeds and code efficiency should remedy this within the next year or two.

Future Trends In HSP And HSP Modems

Advances are already underway to add versatility to existing HSP products. As an example, we can expect to see the addition of a modem chip set that communicates with its host via an on-chip universal serial bus (USB) connection some time near the end of 1997. Cellular data applications will benefit from the inclusion of the MNP-10 protocol into the HSP code later this year. Specifically designed for the challenges posed by the wireless environment, MNP-10 aggressively

handles error correction/detection to reduce bandwidth-robbing re-transmits. As HSP technology evolves, it will be called upon to go beyond simple POTS modem solutions.

With faster platforms and more efficient algorithms, it will soon be possible to support other modulation schemes used in ISDN and asymmetric digital subscriber line (ADSL) connections. ISDN should not represent a significant challenge, since the phase/amplitude modulation and 2B1Q line coding it employs is fairly straightforward. ADSL however, presents some challenges. The ADSL specification permits the use of either discrete multitone (DMT), carrierless amplitude/phase (CAP), or QAM modulation. CAP and QAM-based HSP modems are fairly straightforward, except for their higher data rates (up to 2 Mbits/s downstream). The more complex DMT modulation scheme however, will probably require advances both in CPU speed and HSP processing algorithms before they can be realized on a consumer-grade computer. Nevertheless, it is quite conceivable that we will see a an HSP modem supporting DMT within the next two to three years.

Conclusions

As the expectations for ever-better price and performance in computer equipment steadily rise, engineers will be able to meet them with HSP technology. In some areas, HSP may become the solution of choice simply because it enables users to track communications standards as they evolve via "soft upgrades". Already, HSP has garnered a significant fraction of the consumer PC, laptop, and palmtop computer market. Acceptance should continue to swell into the remainder of the market as its flexibility, power efficiency, and adaptability become better understood within the engineering community.