STANDARD
MICROSYSTEMS
CORPORATION

USB97CFDC

USB Floppy Disk Controller

FEATURES

- 3.3 Volt, Low Power Operation
- Complete USB Specification 1.1 Compatibility
  - Includes USB Transceiver
  - Based on an Enhanced Version of SMSC's Industry Proven USB97C100 USB Controller
- Complete System Solution Including USB Mass Storage Class Compliant Win98/2000 Driver and Firmware
  - Supports 640K, 720K, 1.44M, 1.2M Windows 98 J, and 1.2M NEC DOS 6.x Formats
  - Supports Both the UFI and SFF8070i Command Sets
  - Supports USB Mass Storage Compliant Bootable Floppy BIOS
  - 4ms Seek Times
  - USB 1.1 Compliance, Including Low Power Device Class SUSPEND Mode Operation and Power Control of Disk Drive
  - Disk Drive Feedback of Readiness Upon Power Re-Application Option
  - Option for Ultra High Performance Using Additional Caching SRAM
  - Support for Floppy Drive Power Control
- Contains SMSC's Industry Proven Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Supports Single Normal or Three Mode Floppy Drives
  - Supports Vertical Recording Format and High Capacity Drives in User Written Firmware Applications
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
- Enhanced Digital Data Separator
  - 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Intelligent Auto Power Management
  - <300µA SUSPEND Current
  - <75mA Operating Current
- External Program Memory Interface
  - 32K Byte Code Space (Supplied Firmware Requires 16KB Memory)
  - Flash, SRAM, or EPROM Memory
- 4KB Internal Buffer SRAM for High Performance Operation
- Optional External Cylinder Cache Memory
  - Up to 16K x 8 External SRAM may be Used for Ultra High Performance Applications
- On Board 14.318 MHz Crystal Driver Circuit
- 100 Pin TQFP Package

GENERAL DESCRIPTION

The USB97CFDC is an integration of the USB97C102 Enhanced Multi-Endpoint USB Peripheral Controller, without its integrated hub functions, and the SMSC Floppy Disk Controller used in many of its Super IO products, such as the FDC37C869. Special care in the interconnection of the two devices has been taken to assure the lowest possible system current draw (<300µA) during SUSPEND mode operation.

Provisions for external Flash Memory up to 32K bytes for program storage is provided.

Although not required for standard floppy operation, provisions for 16K bytes of external buffer SRAM, in addition to that included in the USB97C102 core, is also provided for extended applications, such as tape drives and for other special applications is also provided.

Several pins are provided for controlling external power control elements and sensing specialized drive functions.

NOTE: SMSC has developed and supplies firmware and drivers for this device to implement a standard three mode or dual mode Floppy Disk Drive system with drive power control. If the customer desires to develop his own firmware and/or drivers for this system, he may contact SMSC to obtain a complete engineering specification which details all the internal block functions and register maps of the USB97CFDC to allow custom programs to be written for this device.

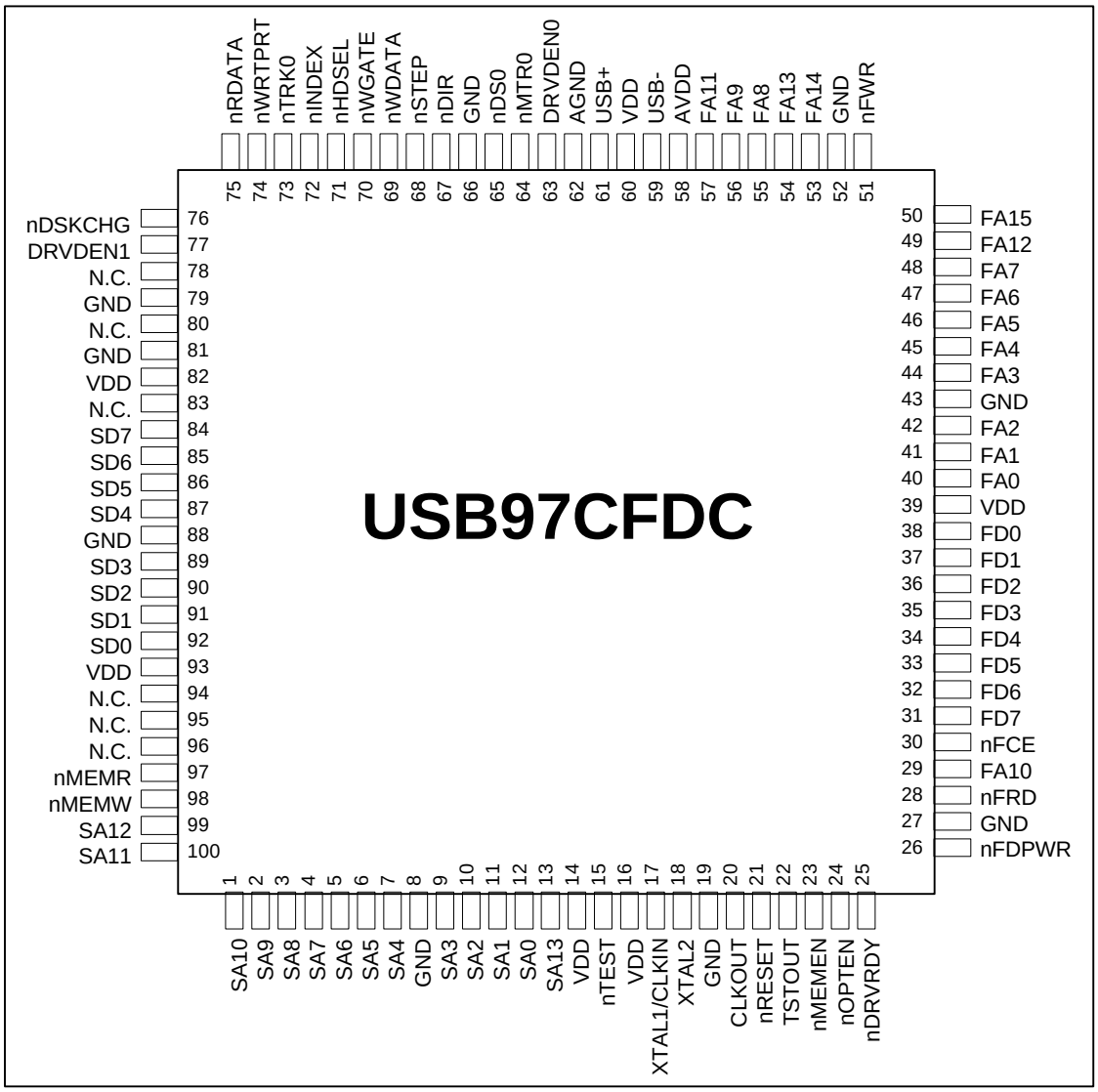
TABLE OF CONTENTS

80 Arkay Drive
Hauppauge, NY 11788
(516) 435-6000
FAX (516) 273-3123

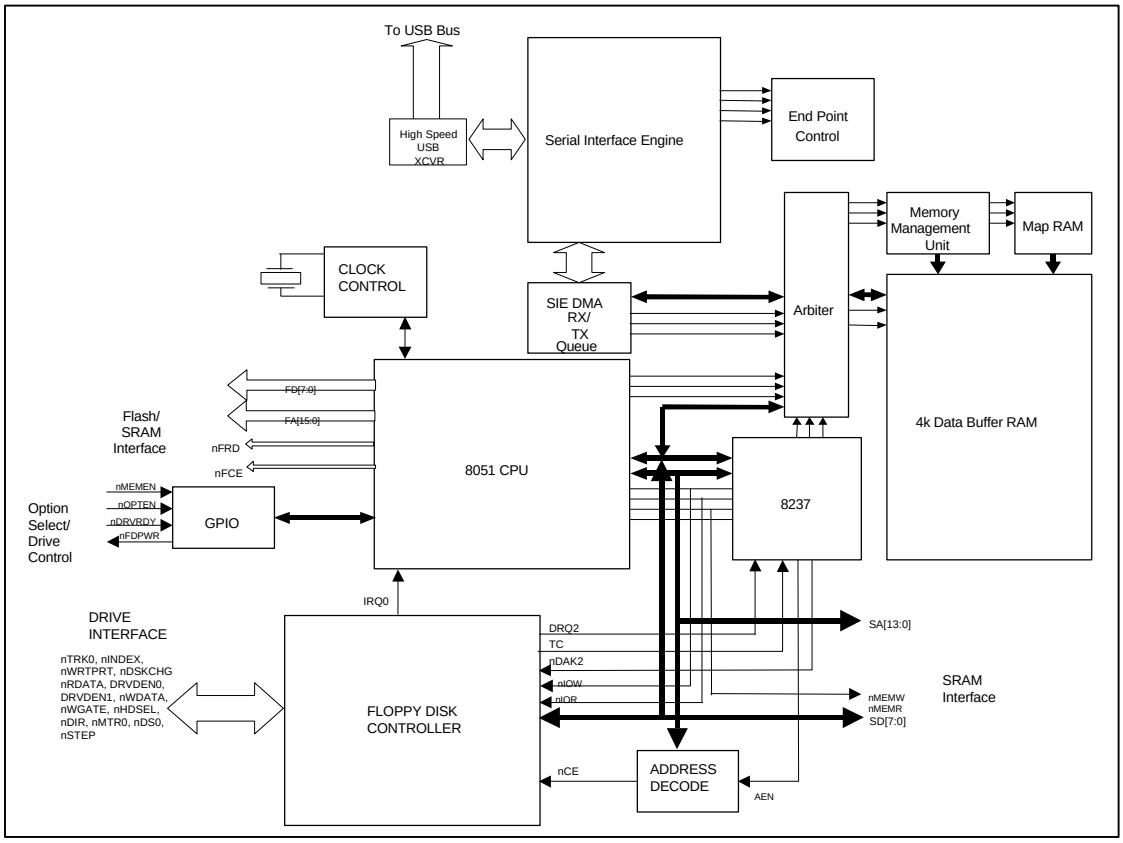
DESCRIPTION OF PIN FUNCTIONS

FLOPPY DISK INTERFACE (14 Pins)			
nTRK0	nINDEX	nWRTPRT	nDSKCHG
nRDATA	DRVDEN0	DRVDEN1	nSTEP
nWDATA	nWGATE	nHDSEL	nDIR
nDSO	nMTR0		
USB INTERFACE (4 Pins)			
USBD+	USBD-	AVDD	AGND
FLASH ROM INTERFACE (27 Pins)			
FD0	FD1	FD2	FD3
FD4	FD5	FD6	FD7
FA0	FA1	FA2	FA3
FA4	FA5	FA6	FA7
FA8	FA9	FA10	FA11
FA12	FA13	FA14	FA15
nFRD	nFCE	nFWR	
SRAM/IO INTERFACE (24 Pins)			
SD0	SD1	SD2	SD3
SD4	SD5	SD6	SD7
SA0	SA1	SA2	SA3
SA4	SA5	SA6	SA7
SA8	SA9	SA10	SA11
SA12	SA13	nMEMR	nMEMW
MISC (10 Pins)			
nMEMEN	OPTEN	nDRVRDY	nFDPWR
XTAL1/CLKIN	XTAL2	nRESET	nTEST
TST_OUT	CLKOUT		
POWER, GROUNDS, and NO CONNECTS (25 Pins)			

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
FLOPPY DISK INTERFACE				
75	Read Disk Data	nRDATA	IS	Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data.
69	Write Data	nWDATA	OD12	This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.
71	Head Select	nHDSEL	OD12	This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed.
67	Direction Control	nDIR	OD12	This high current low active output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion.
68	Step Pulse	nSTEP	OD12	This active low high current driver issues a low pulse for each track-to-track movement of the head.
76	Disk Change	nDSKCHG	IS	This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection.
63	DRVDEN 0	DRVDEN 0	OD12	An active low on this pin indicates a disk drive spindle speed change from 300 RPM to 360 RPM or 1.2M format disks in three mode drives. This pin should be tied to the disk drives spindle speed control input pin.
77	DRVDEN 1	DRVDEN1	OD12	Reserved for future use.
70	Write Gate	nWGATE	OD12	This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
73	Track 0	nTRK0	IS	This active low Schmidt Trigger input senses from the disk drive that the head is positioned over the outermost track.
72	Index	nINDEX	IS	This active low Schmidt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
74	Write Protect	nWRTPRT	IS	This active low Schmidt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored.

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
64	Motor On 0	nMTR0	OD12	This active low open drain output selects motor drive 0.
65	Drive Select 0	nDS0	OD12	This active low open drain output selects drive 0.
USB INTERFACE				
59 61	USB Bus Data	USB- USB+	IO-U	These pins connect to the USB data signals through 33 ohm series resistors. The USB+ line should be pulled up with a 5%, 1.5K ohm resistor to indicate that this is a high speed USB device.
58	USB Transceiver Supply	AVDD		This is the 3.3V supply to the internal USB transceiver.
62	USB Transceiver Ground	AGND		This is the supply ground for the internal USB transceiver.
FLASH INTERFACE				
31-38	Flash Memory Data Bus	FD[7:0]	IO8	These signals are used to transfer data between the internal 8051 and the external FLASH program memory.
36, 40-42, 44-50, 53-57	Flash Memory Address Bus	FA[15:0]	O8	These signals address memory locations within the FLASH memory.
28	Flash Memory Read Strobe	nFRD	O8	Flash ROM Read; active low
30	Flash Memory Chip Select	nFCE	O8	Flash ROM Chip Select; active low
SRAM/IO INTERFACE				
1-7, 9-13, 99,100	SRAM Memory Bus	SA[13:0]	O8	These signals provide the memory address to an external SRAM buffer.
84-87, 89-92	SRAM Memory Data Bus	SD[7:0]	I/O8	These signals are used to transfer data to/from the SRAM Memory.
97	SRAM Memory Read Strobe	nMEMR	O8	Memory read; active low This active low signal indicates that data is to be driven onto the data bus by the SRAM. Data will be latched internal to the chip on the rising edge of this signal

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
98	SRAM Memory Write Strobe	nMEMW	O8	Memory write; active low This active low signal indicates to the SRAM to load data from the data bus on its rising edge.
MISCELLANEOUS				
17	Crystal Input/External Clock Input	XTAL1/ CLKIN	ICLKx	14.318Mhz Crystal or clock input. This pin can be connected to one terminal of the crystal or can be connected to an external 14.318Mhz clock when a crystal is not used.
18	Crystal Output	XTAL2	OCLKx	14.318Mhz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL1/CLKIN. It may not be used to drive any external circuitry other than the crystal circuit.
23	SRAM Enable	nMEMEN	O24	An active low signal is output on this pin to enable the optional external SRAM for extended FDC write and read caching for ultra high performance applications.
24	Option Enable	OPTEN	I	An active low signal on this pin enables the supplied firmware to utilize the optional external SRAM for extended FDC write and read caching for ultra high performance applications . A high on this pin disables this firmware option.
25	Drive Ready	nDRVRDY	I	An active low signal on this pin from the floppy disk drive, after DS0 goes active, indicates that the system may activate MTR0. If the drive does not supply this signal, this pin should be tied low.
26	Drive Power	nFDPWR	OD24	This active low signal is intended to activate an external power switch, either in the drive or on the system board, to supply power to the floppy disk drive. It is active whenever the USB97CFDC is not in SUSPEND mode.
21	RESET input	nRESET	IS	This active low signal is used by the system to reset the chip. The active low pulse should be at least 100ns wide.
22	Test output	TSTOUT	O8	This signal is used for testing the chip via an internal XNOR chain. User should leave it unconnected.
15	Test input	nTEST	I	This signal is a manufacturing test pin. It should be tied to VDD for normal operation.

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
Power, Ground, and No Connects				
14, 16, 39, 60, 82, 93		VDD		+3.3V power
8, 19, 27, 43, 52, 66, 79, 81, 88		GND		Ground Reference
20, 22, 51, 83, 94-96		NC		No Connect. These pins should not be connected externally.

BUFFER TYPE DESCRIPTIONS

Table 1 - USB97CFDC Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input
IP	Input 90µA with internal pull-up
IS	Input with Schmidt trigger
O8	Output with 8mA drive
I/O8	Input/output with 8mA drive
OD12	Open drain….12mA sink
O24	Output with 24mA drive
OD24	Open drain….24mA sink
ICLK	Clock input (TTL levels)
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Defined in USB specification

DC PARAMETERS

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range..... 0^{o}C to $+70^{o}$C
Storage Temperature Range.....-55^{o} to $+150^{o}$C
Lead Temperature Range (soldering, 10 seconds) ..... $+325^{o}$C
Positive Voltage on any pin, with respect to Ground (Note 1) ..... V_{cc}+0.3V
Negative Voltage on any pin, with respect to Ground..... -0.3V
Maximum V_{cc}..... +3.6V
Note 1: Maximum voltage on IS inputs, OD12 and OD24 outputs for floppy disk drive interface is 5.25V

*Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C - 70°C, V_{cc} = +3.3 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.2			V	
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	uA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	uA	V_{IN} = V_{CC}
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4 mA
Output Leakage	I_{OL}	-10		+10	UA	V_{IN} = 0 to V_{CC} (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I/O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	IOL = 8mA
High Output Level	V_{OH}	2.4			V	IOH = -4mA
Output Leakage	I_{OL}	-10		+10	µA	VIN = 0 to Vcc (Note 1)
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	IOL = 12mA
Output Leakage	I_{OL}	-10		+10	µA	VIN = 0 to Vcc (Note 1)
O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	IOL = 24mA
High Output Level	V_{OH}	2.4			V	IOH = -12mA
Output Leakage	I_{OL}	-10		+10	µA	VIN = 0 to Vcc (Note 1)
OD24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	IOL = 24mA
Output Leakage	I_{OL}	-10		+10	µA	VIN = 0 to Vcc (Note 1)
IO-U Note 2						
Supply Current Active	I_{CC}		30	75	MA	All outputs open.
Supply Current Standby	I_{CSBU}		120	300		

Note 1: Output leakage is measured with the current pins in high impedance.
Note 2: See Appendix A for USB DC electrical characteristics.

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 3.3V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

AC PARAMETERS

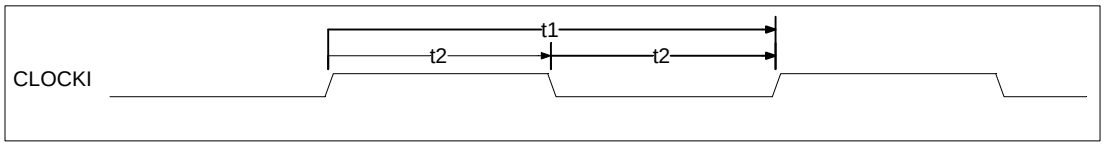


FIGURE 1 - INPUT CLOCK TIMING

TABLE 2 - INPUT CLOCK TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 14.318MHz		69.84		ns
t2	Clock High Time/Low Time for 24MHz	41.9/ 27.9		27.9/ 41.9	ns
t_r, t_f	Clock Rise Time/Fall Time (not shown)			5	ns

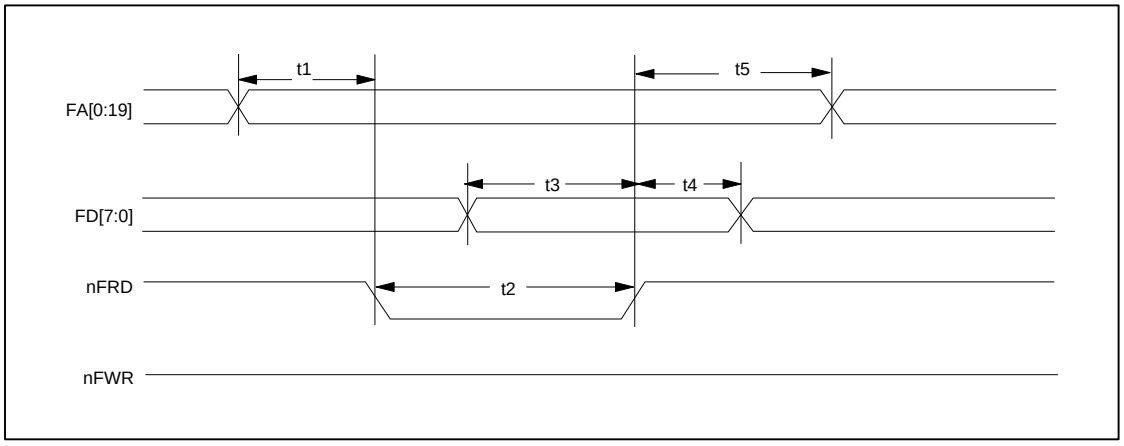


FIGURE 2 – FLASH READ TIMING

TABLE 3 - FLASH READ TIMING

	PARAMETER	MIN	TYP	MAX	UNITS
t1	FA[14:0] Address setup time to nFRD asserted	40			ns
t2	nFRD pulse width	110			ns
t3	FD[7:0] Data setup time to nFRD de-asserted	30			ns
t4	FD[7:0] Data hold time from nFRD de-asserted	0			ns
t5	FA[14:0] Address hold time from nFRD de-asserted	35			ns

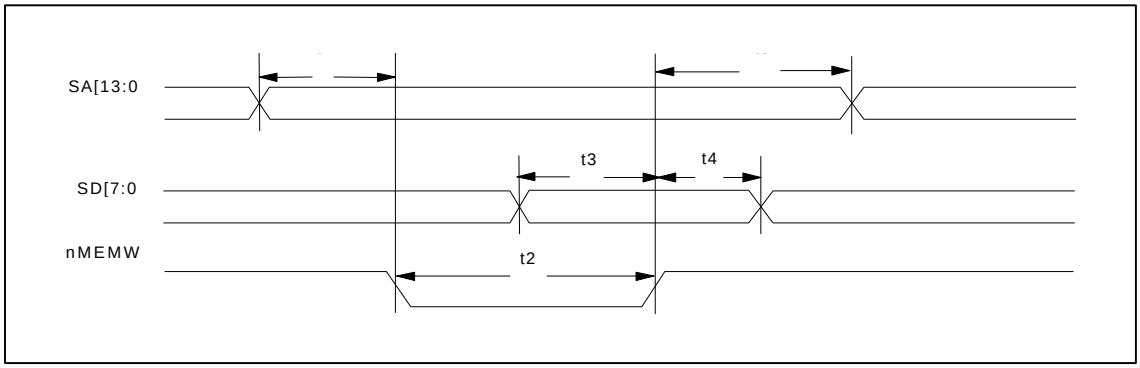


FIGURE 3 – SRAM MEMORY WRITE TIMING

TABLE 4 - SRAM MEMORY WRITE TIMING

	PARAMETER	MIN	TYP	MAX	UNITS
t1	SA[19:0] valid before nMEMWR asserted	10			ns
t2	nMEMWR pulse width	100			ns
t3	SD[7:0] Data setup time to nMEMWR de-asserted	50			ns
t4	SD[7:0] Data hold time from nMEMWR de-asserted	10			ns
t5	nMEMWR de-asserted to SA[13:0] invalid	10			ns

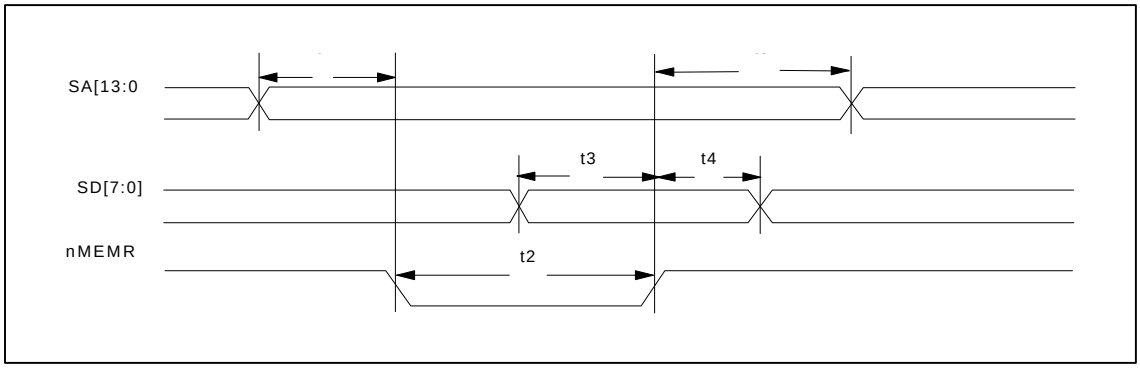
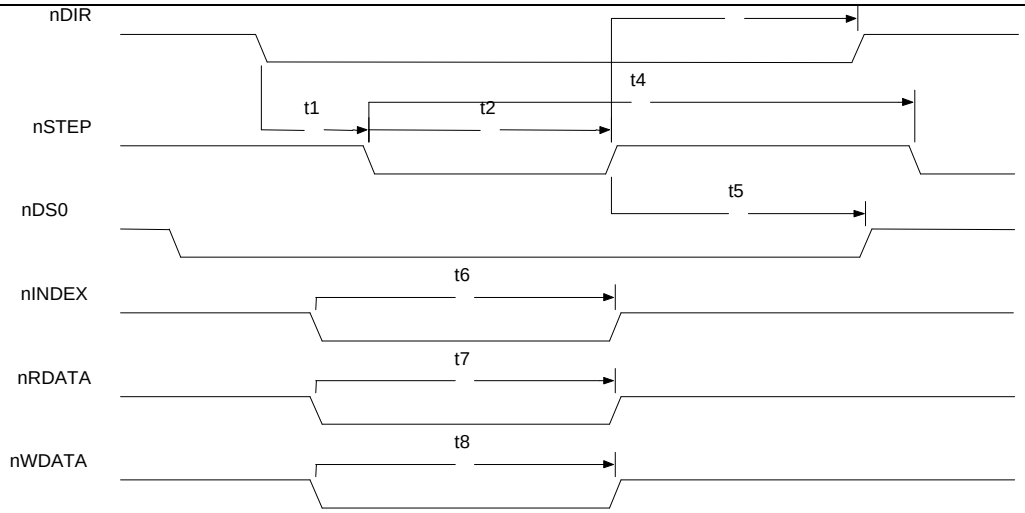


FIGURE 4 - SRAM MEMORY READ TIMING

TABLE 5 - SRAM MEMORY READ TIMING

	PARAMETER	MIN	TYP	MAX	UNITS
t1	SA[19:0] valid before nMEMRD asserted	10			ns
t2	nMEMRD pulse width	100			ns
t3	SD[7:0] Data setup time to nMEMRD de-asserted	50			ns
t4	SD[7:0] Data hold time from nMEMRD de-asserted	20			ns
t5	nMEMRD de-asserted to SA[13:0] invalid	10			ns



	Parameter	min	typ	max	units
t1	nDIR Set Up to nSTEP Low		4		X*
t2	nSTEP Active Time Low		24		X*
t3	nDIR Hold Time After nSTEP		96		X*
t4	nSTEP Cycle Time		132		X*
t5	nDS0-1 Hold Time from nSTEP Low		20		X*
t6	nINDEX Pulse Width		2		X*
t7	nRDATA Active Time Low		40		ns
t8	nWDATA Write Data Width Low		.5		Y*

*X specifies one MCLK period and Y specifies one WCLK period.
MCLK = 16x Data Rate (at 500 Kbp/s MCLK = 8 MHz)
WCLK = 2x Data Rate (at 500 Kbp/s WCLK = 1 MHz)

FIGURE 5 - DISK DRIVE TIMING

USB PARAMETERS

The following tables and diagrams were obtained from the USB specification

USB DC PARAMETERS

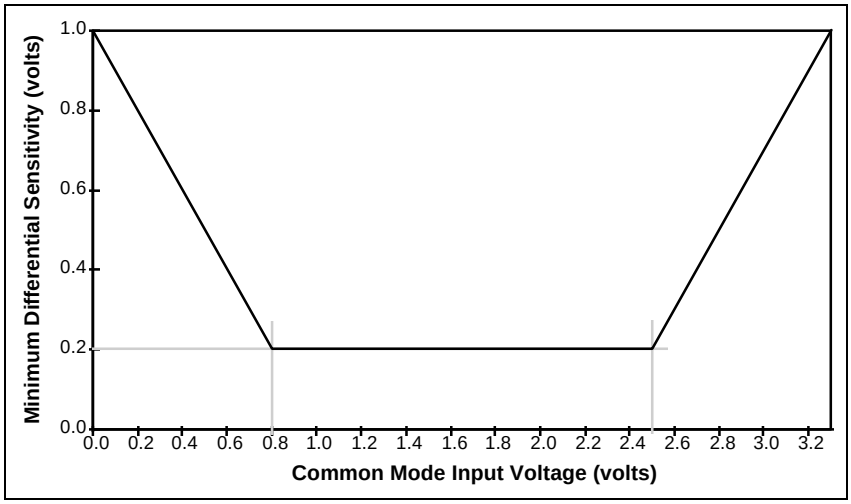


FIGURE 6 - DIFFERENTIAL INPUT SENSITIVITY OVER ENTIRE COMMON MODE RANGE

Table 6 - DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	MIN	TYP	MAX	UNIT
Supply Voltage						
Powered (Host or Hub) Port	VBUS		4.4		5.25	V
Supply Current						
Function	ICC	Note 4			100	mA
Un-configured Function (in)	ICCINIT	Note 5			100	uA
Suspend Device	ICCS				100	uA
Leakage Current						
Hi-Z State Data Line Leakage	ILO	0 V < VIN < 3.3 V	-10		10	uA
Input Levels						
Differential Input Sensitivity	VDI	|(D+) - (D-)|, and FIGURE 6	0.2			V
Differential Common Mode Range	VCM	Includes VDI range	0.8		2.5	V

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	MIN	TYP	MAX	UNIT
Single Ended Receiver Threshold	VSE		0.8		2.0	V
Output Levels						
Static Output Low	VOL	RL of 1.5 KΩ to 3.6 V			0.3 (3)	V
Static Output High	VOH	RL of 15 KΩ to GND	2.8		3.6 (3)	V
Capacitance						
Transceiver Capacitance	CIN	Pin to GND			20	pF
Terminals						
Bus Pull-up Resistor on Root Port	RPU	(1.5 KΩ +/- 5%)	1.425		1.575	kΩ
Bus Pull-down Resistor on Downstream Port	RPD	(15 KΩ +/- 5%)	14.25		15.75	kΩ

Note 1: All voltages are measured from the local ground potential, unless otherwise specified.
Note 2: All timing use a capacitive load (CL) to ground of 50pF, unless otherwise specified.
Note 3: This is relative to VUSBIN.
Note 4: This is dependent on block configuration set by software.
Note 5: When the internal ring oscillator and waiting for first setup packet.

USB AC PARAMETERS

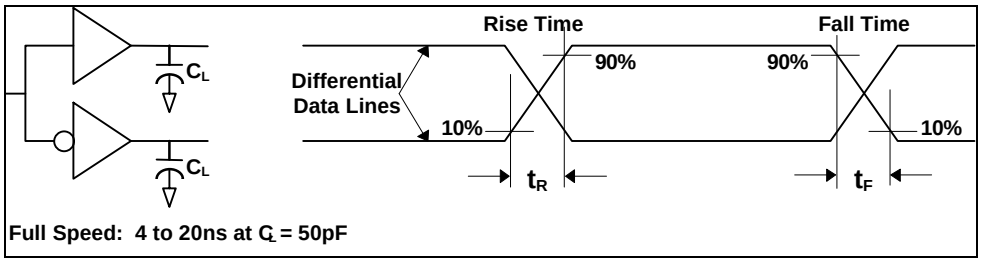


FIGURE 7 - DATA SIGNAL RISE AND FALL TIME

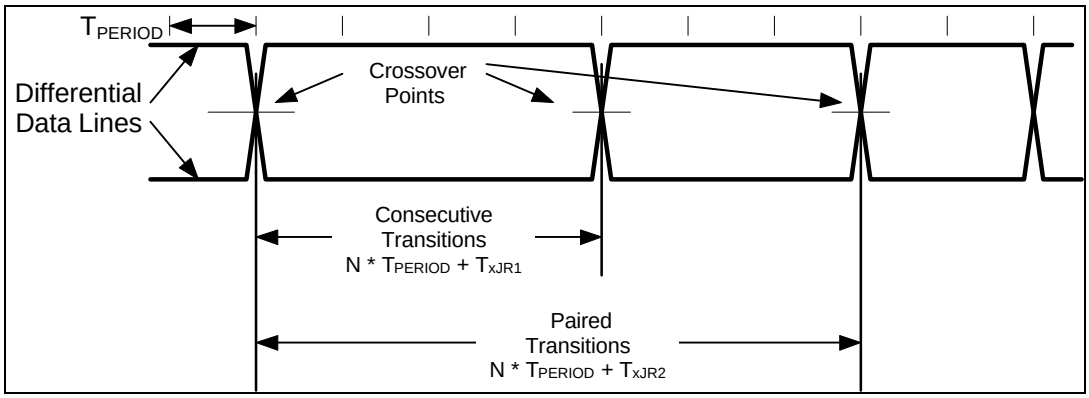


FIGURE 8 - DIFFERENTIAL DATA JITTER

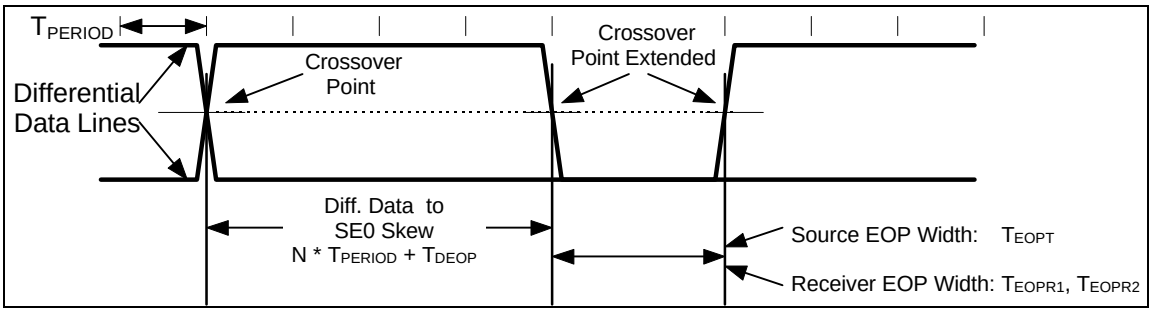


FIGURE 9 - DIFFERENTIAL TO EOP TRANSITION SKEW AND EOP WIDTH

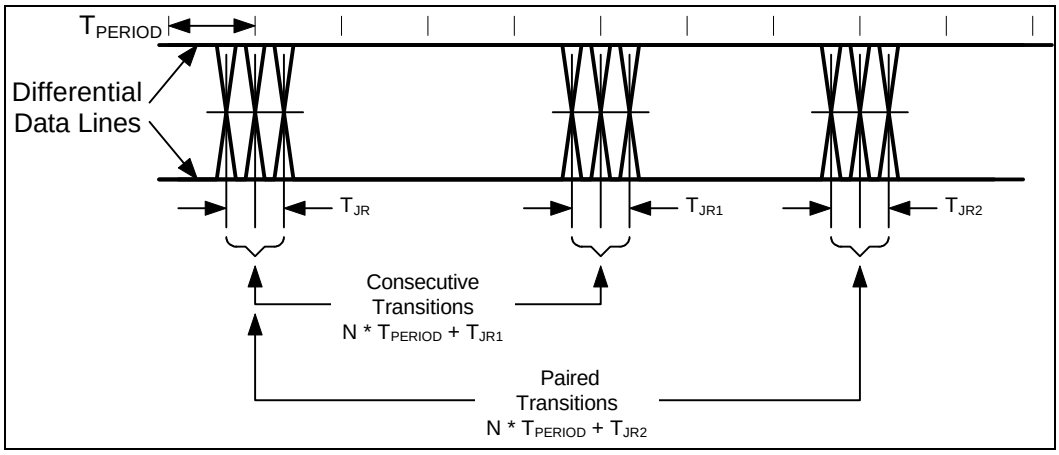


FIGURE 10 - RECEIVER JITTER TOLERANCE

Table 7 - Full Speed (12Mbps) Source Electrical Characteristics

PARAMETER	SYM	CONDITIONS (NOTE 1, 2, 3)	MIN	TYP	MAX	UNIT
Driver Characteristics:						
Transition Time: Rise Time Fall Time	 TR TF	Note 4,5 and FIGURE 7 CL = 50 pF CL = 50 pF	 4 4		 20 20	 ns ns
Rise/Fall Time Matching	TRFM	(TR/TF)	90		110	%
Output Signal Crossover Voltage	VCRS		1.3		2.0	V
Drive Output Resistance	ZDRV	Steady State Drive	28		43	Ω
Data Source Timing:						
Full Speed Data Rate	TDRATE	Ave. Bit Rate (12 Mb/s +/- 0.25%) Note 8	11.95		12.03	Mbs
Frame Interval	TFRAME	1.0 ms +/- 0.05%	0.9995		1.0005	ms
Source Differential Driver Jitter To next Transition For Paired Transitions	 TDJ1 TDJ2	Note 6, 7 and FIGURE 8	 -3.5 -4.0		 3.5 4.0	 ns ns
Source EOP Width	TEOPT	Note 7 and FIGURE 9	160		175	ns

PARAMETER	SYM	CONDITIONS (NOTE 1, 2, 3)	MIN	TYP	MAX	UNIT
Differential to EOP transition Skew	TDEOP	Note 7 and FIGURE 9	-2		5	ns
Receiver Data Jitter Tolerance		Note 7 and FIGURE 10				
To next Transition	TJR1		-18.5		18.5	ns
For Paired Transitions	TJR2		-9		9.0	ns
EOP Width at receiver		Note 7 and FIGURE 9				
Must reject as EOP	TEOPR1		40			ns
Must Accept	TEOPR2		82			ns
Cable Impedance and Timing						
Cable Impedance (Full Speed)	ZO	(45 Ω +/- 15%)	38.75		51.75	Ω
Cable Delay (One Way)	TCBL				30	ns

Note 1: All voltages are measured from the local ground potential, unless otherwise specified.
Note 2: All timing use a capacitive load (CL) to ground of 50pF, unless otherwise specified.
Note 3: Full speed timings have a 1.5KΩ pull-up to 2.8 V on the D+ data line.
Note 4: Measured from 10% to 90% of the data signals.
Note 5: The rising and falling edges should be smoothly transiting (monotonic).
Note 6: Timing differences between the differential data signals.
Note 7: Measured at crossover point of differential data signals.
Note 8: These are relative to the 14.318 MHz crystal.

MECHANICAL OUTLINE

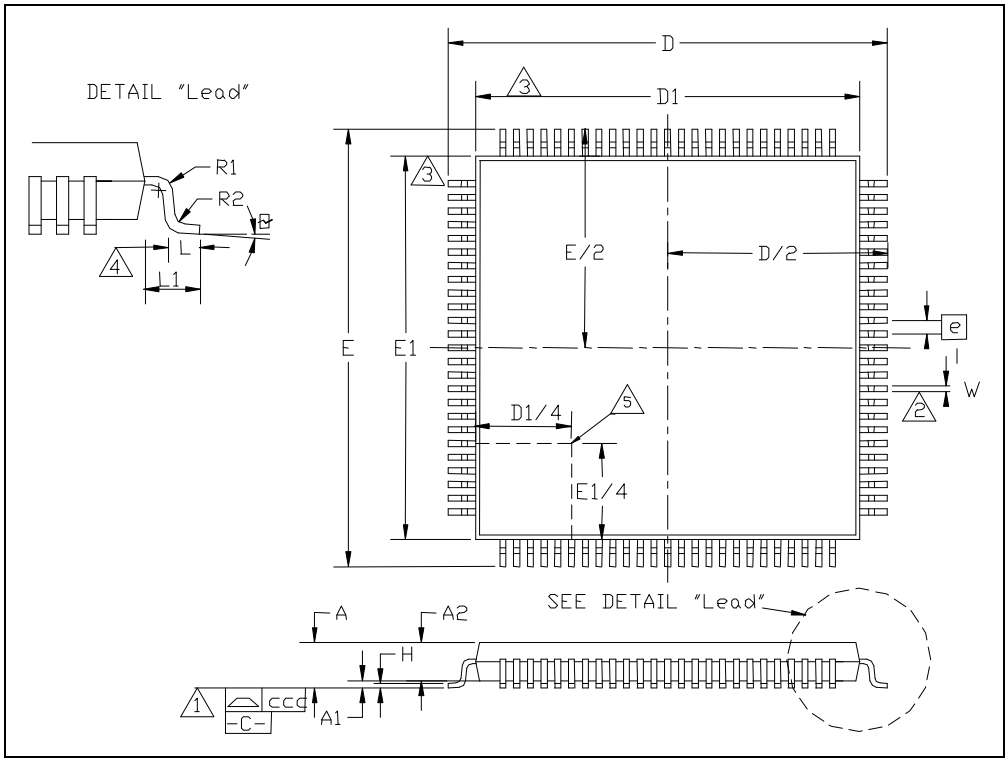


FIGURE 11 - 100 PIN TQFP PACKAGE

See Table on the following page.

	MIN	NOMINAL	MAX	REMARK
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	1.40	1.45	Body Thickness
D	13.80	14.00	14.20	X Span
D/2	6.90	7.00	7.10	$^1/_2$ X Span Measure from Centerline
D1	11.80	12.00	12.20	X body Size
E	13.80	14.00	14.20	Y Span
E/2	6.90	7.00	7.10	$^1/_2$ Y Span Measure from Centerline
E1	11.80	12.00	12.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length from Centerline
L1	~	1.00	~	Lead Length
e		0.40 Basic		Lead Pitch
	0^o	3.5^o	7^o	Lead Foot Angle
W	0.13	0.16	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

Note 1: Controlling Unit: millimeter

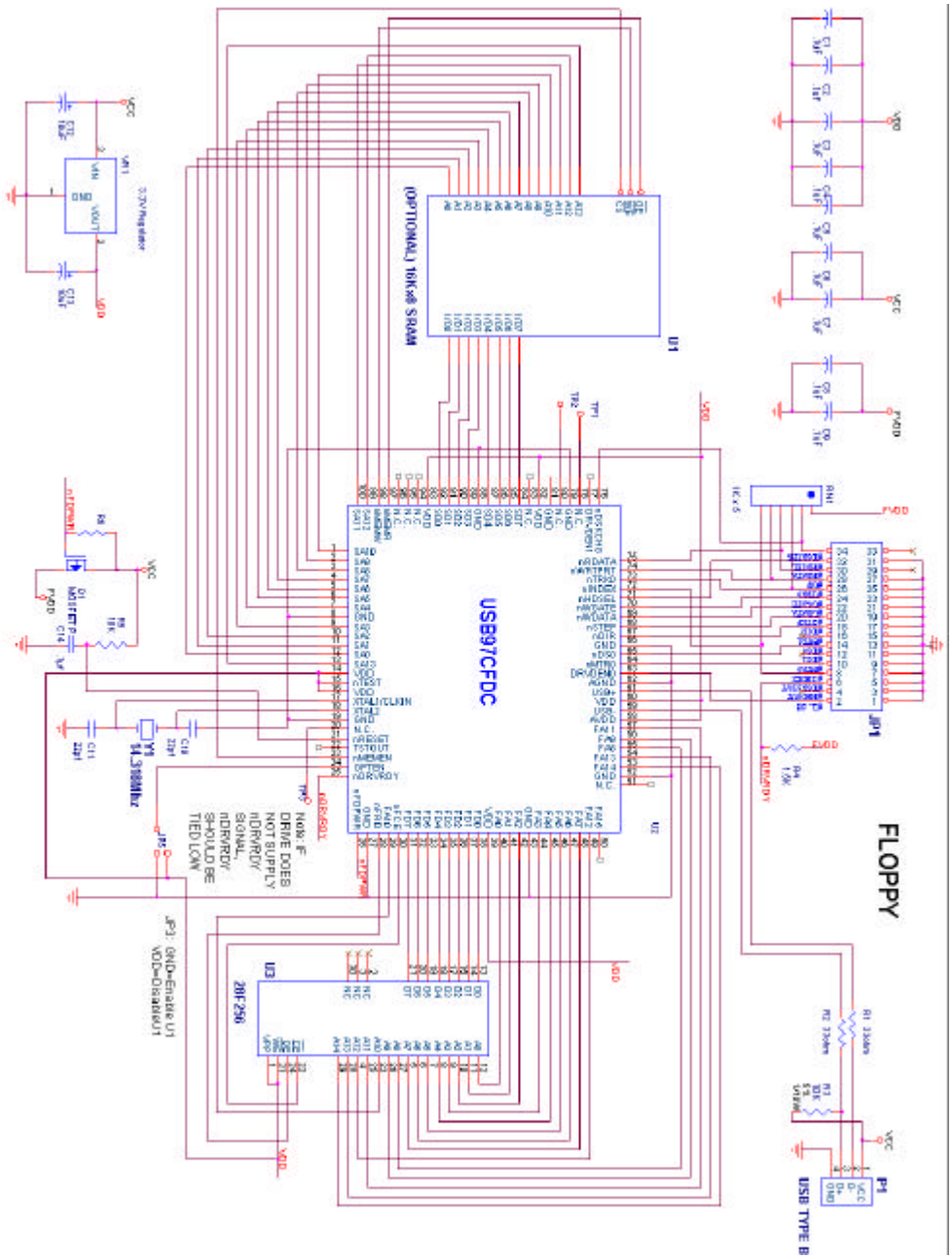
Note 2: Minimum space between protrusion and an adjacent lead is .007 mm.

Note 3: Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm

Note 5: Details of pin 1 identifier are optional but must be located within the zone indicated.

APPENDIX A:

USB97CFDC TYPICAL APPLICATION



SMSC Provided Software for USB97CFDC

SMSC provides the following for the USB97CFDC:

I. Program firmware with the following features:
   (a) Supports 640K, 720K, 1.44M, 1.2M Windows J, 1.2M NEC DOS 6.x formats.
   (b) Supports both the UFI and CBI command sets.
   (c) Supports USB Mass Storage compliant bootable floppy BIOS.
   (d) 4ms Seek times.
   (e) USB 1.1 compliance, including low power device class SUSPEND mode operation and power control of disk drive.
   (f) Disk drive feedback of readiness upon power re-application.
   (g) Option for ultra high performance using additional caching SRAM.

II. USB Mass Storage Class compliant, CBI command set driver for Windows 98.

Circuit diagrams utilizing SMSC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any licenses under the patent rights of SMSC or others. SMSC reserves the right to make changes at any time in order to improve design and supply the best product possible. SMSC products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of SMSC and further testing and/or modification will be fully at the risk of the customer.

USB97CFDC Rev. 05/25/99