Design Considerations for Migrating from an 8x930 to an 8x931 USB Peripheral Controller

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1.0 About This Document

This document describes both hardware and software issues that should be considered when migrating from Intel's 8*x*930HF/HG to an 8*x*931HA or from the 8x930AD/AE to an 8x931AA Universal Serial Bus peripheral controllers. All device references in this document will be made to the 8x930 and 8x931 unless it applies to a specific device. Customers need to perform thorough validation of their application hardware and software once making the migration and prior to production.

1.1 Additional Information Sources

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

Intel Corporation
Literature Sales
PO Box 5937
Denver, CO 80217-9808
1-800-548-4725

or find a variety of technical and product information through Intel's World Wide Web (WWW) location at:

http://www.intel.com/design/usb/

Table 1. Related Documentation

Document Title	Order Number
8x931AA***, 8x***931HA ***Universal Serial Bus Peripheral Controller User's Manual, Rev. 1.0***	273102-001
8x931AA***, 8x***931HA ***Universal Serial Bus Peripheral Controller Data Sheet, Rev. 1.0***	273108-001
8x931AA***, 8x***931HA ***Universal Serial Bus Peripheral Controller Specification Update***	273140-001

2.0 CPU Core Change

The 8*x*931 uses the MCS®51 microcontroller core, so there are some basic differences from the 8*x*930 that need to be considered; including the instruction set, register file, speed, and ICC.

To ease in the migration process, make sure the 8*x*930 code contains only MCS 51 architecture (accumulator-based) instructions. The 8*x*931 does not execute MCS®251 architecture (register-based) instructions. Therefore, you must convert any MCS 251 architecture instructions to MCS 51 architecture instructions for use with the 8*x*931 peripheral controller.

Note: *The easiest approach may be to use a MCS 51 microcontroller assembler to automatically flag the MCS 251 microcontroller instructions, instead of manually changing them line-by-line.*

The 8*x*931 uses a 12MHz external clock (XTAL1) which generates a 6MHz internal clock (Fclk) for the CPU and peripherals. The 8*x*931 CPU executes single-cycle instructions in one machine cycle (six states of 2 Tosc per state).

Notice that the following DC specifications are different for the 8*x*931: Iil, Rrst, Ipd, Idl, Icc. Also all AC specifications have changed.

3.0 Removal of PCA and WDT Peripherals

The 8*x*931 does not include two standard MCS 51 architecture peripherals; Programmable Counter Array (PCA) and Watchdog Timer (WDT). All special function registers (SFRs), interrupts and pins associated with these peripherals are not available on the 8*x*931. Therefore, if your 8*x*930 application uses these peripherals, an alternate solution must be used when migrating to the 8*x*931 controller.

4.0 Memory Partitioning and Addressing

The 8*x*931 controller has 8Kbytes of on-chip ROM and 256 bytes of on-chip RAM. If your application exceeds these boundaries, then external memory components can be used. Note that the MCS 51 architecture used by the 8*x*931 has separate 64-Kbyte address spaces for program memory and data memory, instead of the single 256-Kbyte address space employed by the MCS 251 architecture.

The 8*x*930 controller allows all SFRs to be bit-addressable, while the 8*x*931 allows only SFRs with addresses ending in 0H or 8H to be bit-addressable. Therefore, all bit instructions (i.e. SETB, CLR, etc.) used for the wrong SFR addresses will need to be changed to logical-OR or logical-AND instructions.

5.0 Pinout Changes

Table 2 lists the pinout differences between the 8*x*930HF/HG and 8*x*931HA for the 68-pin PLCC package; all other pins remain the same. Table 3 lists the pinout differences between the 8*x*930Ax and the 8*x*931AA for the 68-pin PLCC package; all other pins remain unchanged.

Table 2. 68-Pin PLCC Package

Pin #	**8*x*930HF/HG**	8*x*931HA
20	P3.0/RXD	P3.0/OVRI#
21	P3.1/TXD	P3.1/SOF#
34	P1.6/CEX3/WAIT#	P1.6/RXD
35	P1.7/CEX4/A17/WCLK	P1.7/TXD
36	Vcc	LED3
37	Vss	LED2
43	PLLSEL2	LED1
44	PLLSEL0	LED0
47	Reserved	Vss
50	SOF#	Vss
56	Reserved	Vcc
57	DM1	DM5
58	DP1	DP5
59	DM5	DM4
60	DP5	DP4
61	OVRI#	Reserved
62	UPWEN#	Reserved
63	Reserved	Vss
64	Reserved	UPWEN#

NOTES:
1. To design a board that supports both the 8*x*930HF/HG and 8*x*931HA, you can use jumpers for the pinout differences.
2. Pin 42 is PLLSEL1 for the 8*x*930HF/HG and PLLSEL for the 8*x*931HA. This pin should be pulled high for full speed USB data rate of 12Mbps. Therefore, no hardware change required.
3. Pins 57, 58, 59 and 60 have changed port numbering, but this should not result in any hardware changes.
4. Pin function additions or deletions due to different feature sets are assumed and are not listed in this table (i.e., KSO,KSI, wait state, A16 and A17).

Table 3. 68-Pin PLCC Package

Pin #	**8*x*930**Ax	8*x*931AA
20	P3.0/RXD	P3.0
21	P3.1/TXD	P3.1/SOF#
34	P1.6/CEX3/WAIT#	P1.6/RXD
35	P1.7/CEX4/A17/WCLK	P1.7/TXD
36	Vcc	LED3
37	Vss	LED2
42	PLLSEL1	PLLSEL
43	PLLSEL2	LED1
44	PLLSEL0	LED0
47	Reserved	Vss
50	SOF#	Vss
56	Reserved	Vcc
63	Reserved	Vss
64	Reserved	FSSEL

NOTES:
1. To design a board that supports both the 8*x*930Ax and 8*x*931AA, you can use jumpers for the pinout differences.
2. Pin 42 is PLLSEL1 for the 8*x*930Ax and PLLSEL for the 8*x*931AA. This pin may not require a hardware change, if the USB data rate is already appropriately selected.
3. Pin function additions or deletions due to different feature sets are assumed and are not listed in this table (i.e., KSO,KSI, wait state, A16 and A17).

6.0 Size and Number of Function FIFOs

The 8*x*931 provides three function endpoint pairs. The 8*x*931 function endpoint transmit/receive FIFOs are smaller than the 8*x*930 FIFOs. The 8*x*931 function FIFOs sizes are: endpoint 0 (control)= 8/8bytes, endpoint 1 = 16/16bytes and endpoint 2 = 8/8bytes. Also, endpoint 1 is the only 8*x*931 endpoint that supports isochronous data transfers and dual packet mode. Refer to Table 4.

7.0 Downstream Port Numbering

The 8*x*931HA controller has four external downstream ports. Note that these downstream ports have been renumbered. The internal downstream port still exists on the 8*x*931HA, but its number has changed from USB port 4 on the 8*x*930HF/HG to USB port 1 on the 8*x*931HA. Therefore, firmware must change to make sure the proper port is being accessed via the HPINDEX register. Refer to Table 5.

8.0 SFR Map

The special function registers (SFRs) for the PCA and WDT have been removed but the remaining SFRs, including all USB SFRs, remain in the same locations. The 8*x*931 has one new SFR, KBCON (keyboard control), located at address F8H.

9.0 New Bit Definitions

For the 8*x*931HA device, HSTAT.7 is no longer a reserved bit, it is now defined as OVRIEN. This overcurrent detect enable bit is used to gate off the overcurrent input detect which is multiplexed with P3.0. When set, a low on P3.0/OVRI# pin will trigger overcurrent detection logic. When this bit is '0', the overcurrent detection logic is disabled.

For the 8*x*931, the addition of External Interrupt 2 (keyboard scan interrupt) has changed the definition of some reserved bits. IEN1.7 (EX2) is now defined as the enable bit, and IPL1.7/IPH1.7 are defined as the interrupt priority bits for external interrupt 2.

Table 4. Embedded Function FIFOs

EPINDEX	Endpoint Pair	Transmit FIFOs	Receive FIFOs	USB Data Transfer Type
0000 0000	Function Endpoint 0	8 bytes	8 bytes	Control
0000 0001	Function Endpoint 1	16 bytes	16 bytes	Control, Interrupt, Bulk, Isochronous
0000 0010	Function Endpoint 2	8 bytes	8 bytes	Control, Interrupt, Bulk

Table 5. Downstream Port (DSP) Allocation

DSP #	8*x*930HD/HE	8*x*930HF/HG	8*x*931HA
1	External	External	Internal (EF)
2	External	External	External
3	External	External	External
4	Internal (EF)	Internal (EF)	External
5	—	External	External

NOTE: EF = Embedded Function