E2N0026-18-Y3

Preliminary

OKI Semiconductor

This version: Nov. 1998

ML60851A

USB Device Controller

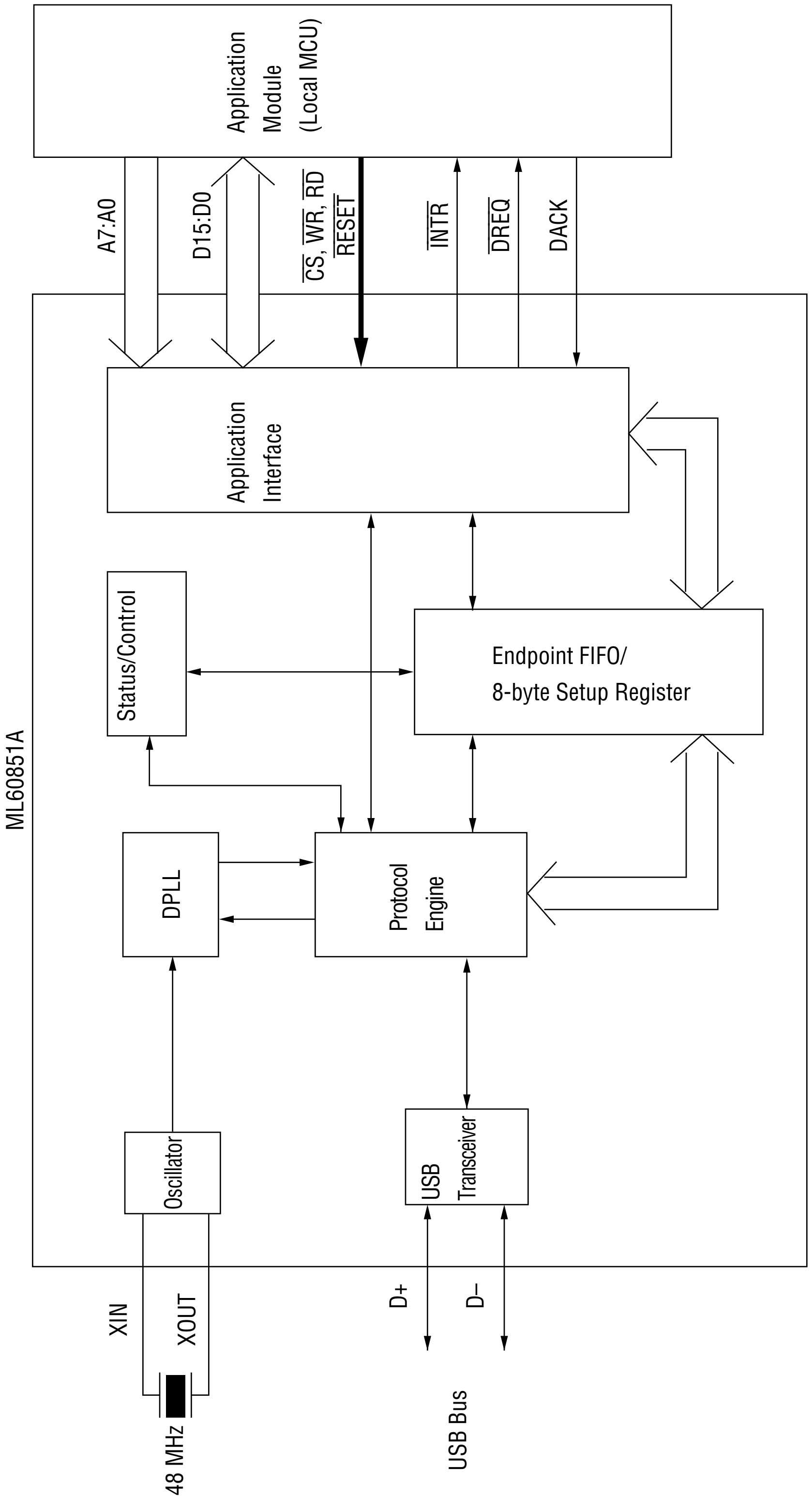
GENERAL DESCRIPTION

The ML60851A is a general purpose Universal Serial Bus (USB) device controller. The ML60851A provides a USB interface, control/status block, application interface, and FIFOs. The FIFO interface and two types of transfer have been optimized for BulkOut devices such as printers and BulkIn devices such as digital still cameras and image scanners. In addition, Mass Storage devices are also applicable to this device.

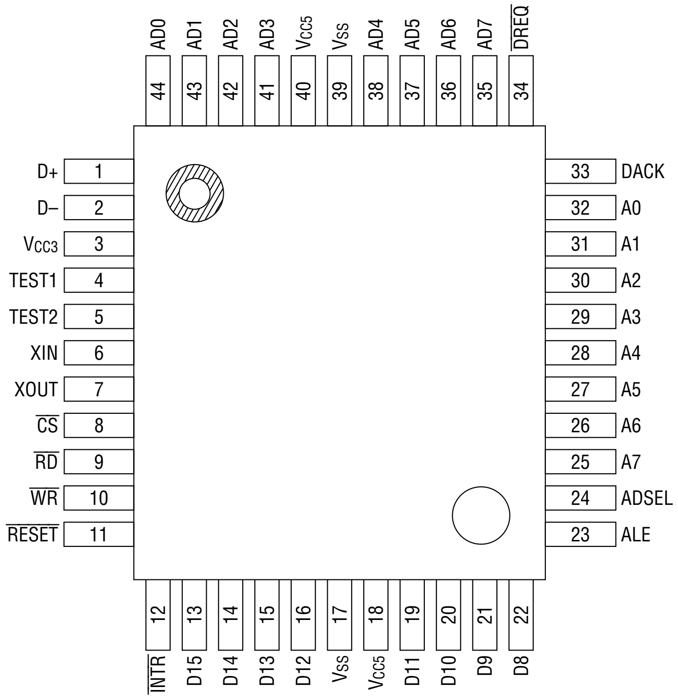
FEATURES

- USB 1.0 compliant
- Built-in USB transceiver circuit
- Full-speed (12 Mb/sec) support
- Supports printer device class, image device class, and Mass Storage device class
- Supports three types of transfer; control transfer, bulk transfer, and interrupt transfer
- Built-in FIFOs for control transfer
  Two 8-byte FIFOs (one for receive FIFO and the other for transmit FIFO)
- Built-in FIFOs for bulk transfer (available for either receive FIFO or transmit FIFO)
  One 64-byte FIFO
  Two 64-byte FIFOs
- Built-in FIFO for interrupt transfer
  One 8-byte FIFO
- Supports one control endpoint, two bulk endpoint addresses, and one interrupt endpoint address
- Two 64-byte FIFOs enable fast BulkOut transfer and BulkIn transfer
- Supports 8 bit/16 bit DMA transfer
- V_{CC} is 3.0 V to 3.6 V
- Supporting dual power supply enables 5 V application interface
- Built-in 48 MHz oscillator circuit
- Package options:
  44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name: ML60851AGA)
  44-pin plastic TQFP (TQFP44-P-1010-0.80-K) (Product name: ML60851ATB)

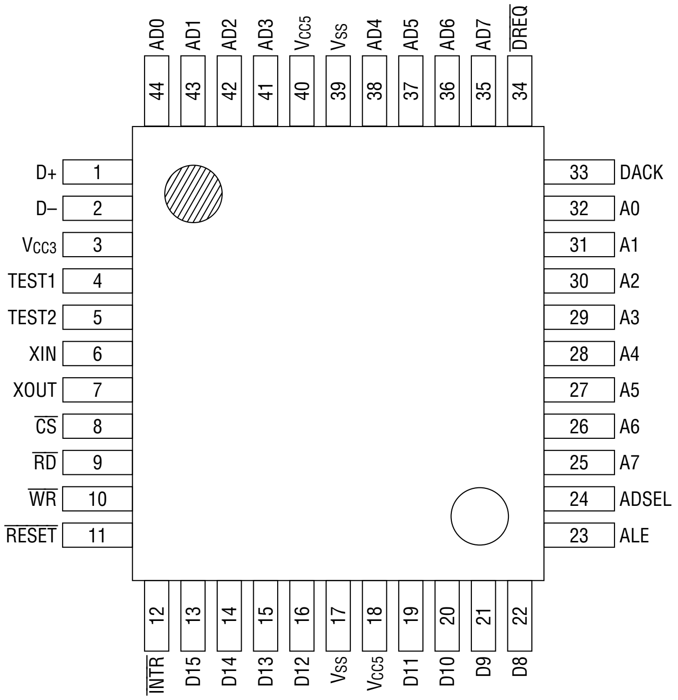
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic QFP



44-Pin Plastic TQFP

PIN DESCRIPTION

Pin	Symbol	Type	Description
1, 2	D+, D–	I/O	USB data
6, 7	XIN, XOUT	—	Pin for external crystal oscillator
4, 5	TEST1, 2	I	Test Pins (normally "L")
13 to 16, 19 to 22	D15:D8	I/O	Data bus (MSB)
35 to 38, 41 to 44	AD7:AD0	I/O	Data bus (LSB)/address input
25 to 32	A7:A0	I	Address input
8	$\overline{\text{CS}}$	I	Chip select signal input pin. LOW active
9	$\overline{\text{RD}}$	I	Read signal input pin. LOW active
10	$\overline{\text{WR}}$	I	Write signal input pin. LOW active
12	$\overline{\text{INTR}}$	O	Interrupt request signal output pin
34	$\overline{\text{DREQ}}$	O	DMA request output pin
33	DACK	I	DMA acknowledge signal input pin
23	ALE	I	Address latch enable signal input pin
24	ADSEL	I	Address input mode select input pin. "H": address/data multiplex
11	$\overline{\text{RESET}}$	I	System Reset signal input pin. LOW active

INTERNAL REGISTERS

Addresses and Names of Registers

Address			Register name
A5:A0	Read A7, A6	Write A7, A6	
00h	11b	01b	Device Address Register
01h	11b	01b	Device State Register
02h	11b	—	Packet Error Register
03h	11b	—	Receive FIFO Register
04h	11b	—	Transmit FIFO Register
08h	11b	01b	Endpoint Packet-Ready Register
09h	11b	—	Endpoint 0 Receive-Byte Count Register
0Ah	11b	—	Endpoint 1 Receive-Byte Count Register
0Bh	11b	—	Endpoint 2 Receive-Byte Count Register
0Eh	—	01b	Flash Transmit FIFO
0Fh	—	01b	System Control
10h	11b	—	bmRequestType Setup Register
11h	11b	—	bRequest Setup Register
12h	11b	—	wValue LSB Setup Register
13h	11b	—	wValue MSB Setup Register
14h	11b	—	wIndex LSB Setup Register
15h	11b	—	wIndex MSB Setup Register
16h	11b	—	wLength LSB Setup Register
17h	11b	—	wLength MSB Setup Register
1Ah	11b	01b	Assertion Select Register
1Bh	11b	01b	Interrupt Enable Register
1Ch	11b	—	Interrupt Status Register
1Dh	11b	01b	DMA Control Register
1Eh	11b	01b	DMA Interval Register
1Fh	—	—	Reserved
20h	11b	—	Endpoint 0 Receive Control Register
21h	11b	—	Endpoint 0 Receive General Register
22h	11b	01b	Endpoint 0 Receive Payload Register
23h	—	—	Reserved
24h	11b	01b	Endpoint 1 Control Register
25h	11b	01b	Endpoint 1 General Register
26h	11b	01b	Endpoint 1 Payload Register
27h	—	—	Reserved

Addresses and Names of Registers (Continued)

Address			Register name
A5:A0	Read A7, A6	Write A7, A6	
30h	11b	—	Endpoint 0 Transmit Control Register
31h	11b	—	Endpoint 0 Transmit General Register
32h	11b	01b	Endpoint 0 Transmit Payload Register
33h	11b	01b	Endpoint 0 General Register
34h	11b	01b	Endpoint 2 Control Register
35h	11b	01b	Endpoint 2 General Register
36h	11b	01b	Endpoint 2 Payload Register
37h	—	—	Reserved
38h	11b	01b	Endpoint 3 Control Register
39h	11b	01b	Endpoint 3 General Register
3Ah	11b	01b	Endpoint 3 Payload Register
00h	01b	—	Endpoint 0 Receive FIFO data
01h	01b	—	Endpoint 1 Receive FIFO data
02h	01b	—	Endpoint 2 Receive FIFO data
00h	—	11b	Endpoint 0 Transmit FIFO data
01h	—	11b	Endpoint 1 Transmit FIFO data
02h	—	11b	Endpoint 2 Transmit FIFO data
03h	—	11b	Endpoint 3 Transmit FIFO data

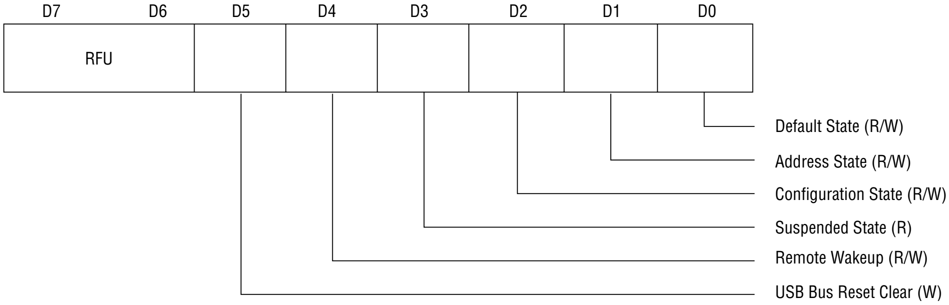
Register Description

Device Address Register (C0h, 40h)

D7	D6	D5	D4	D3	D2	D1	D0
RFU	Device Address (R/W)						

The local MCU writes a device address, which is given by the SET_ADDRESS command form the host computer, into this register. Thereafter, this device processes an only token packet transmitted to the given device address.

Device State Register (C1h, 41h)



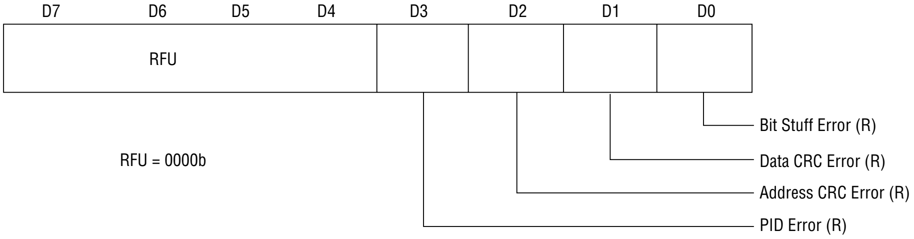
Default, Address, and Configuration States: D2, D1, and D0 are set to 0, 0, and 1 (default states) by reset respectively. Changing the values of this register gives no influence on operation of this device.

Suspended State: This register is asserted when the device enters the suspended state.
This register is deaserted by reset or when the device exits the suspended state by a resume signaling from the USB bus.

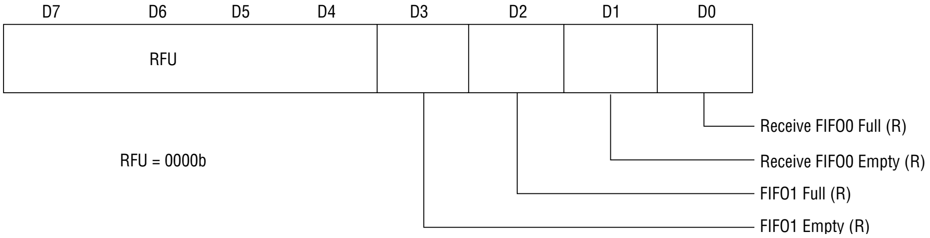
Remote Wakeup: When this device signals a remote wakeup during the suspended state, this register is asserted by a local MCU. This register is automatically deasserted when the device exits the suspended state by a resume signaling from the USB bus.

USB Bus Reset Status Clear: Writing "1" to this bit causes the interrupt status to be cleared (the USB bus reset interrupt status bit is "0" and the $\overline{\text{INTR}}$ pin is deasserted) while the USB bus reset interrupt is being serviced (when D5, the USB bus reset interrupt status bit, of the interrupt status register is "1" and the $\overline{\text{INTR}}$ pin is asserted). This bit is readable, and when read, its value will be always "0".

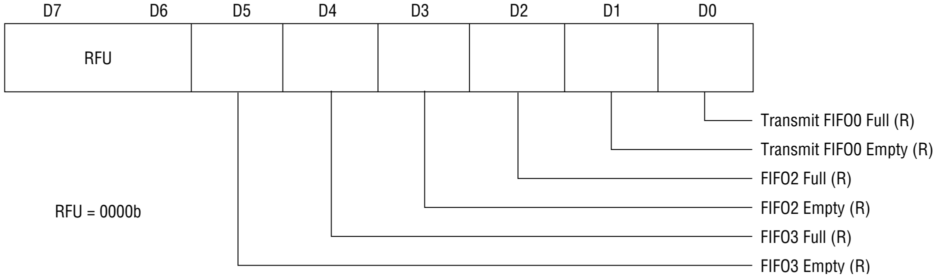
Packet Error Register (C2h, –)



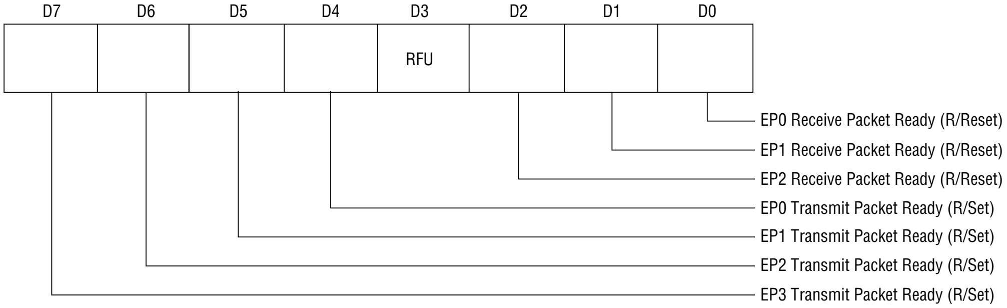
FIFO Status Register 1 (C3h, –)



FIFO Status Register 2 (C4h, –)



Endpoint Packet-Ready Register (C8h, 48h)


D7
D6
D5
D4
D3
D2
D1
D0
RFU
EP0 Receive Packet Ready (R/Reset)
EP1 Receive Packet Ready (R/Reset)
EP2 Receive Packet Ready (R/Reset)
EP0 Transmit Packet Ready (R/Set)
EP1 Transmit Packet Ready (R/Set)
EP2 Transmit Packet Ready (R/Set)
EP3 Transmit Packet Ready (R/Set)

Receive Packet Ready: When a valid packet arrives at an endpoint, this bit is automatically set and the endpoint is locked. When "1" is written in this register, Receiver Packet Ready is reset and the endpoint is unlocked. (This bit also is set to "0".)
When DMA is enabled, EP1 Receive Packet Ready is automatically reset after all the data in EP1 is read during DMA transfer.

Transmit Packet Ready: When "1" is written in this register, the Transmit Packet Ready is set and the packet in the corresponding endpoint is transmitted. Transmit Packet Ready is automatically reset when the ACK handshake is returned from the host.
When DMA is enabled, EP1 Transmit Packet Ready is automatically set after the data written in EP1 reaches the maximum packet size during DMA transfer.

The value of this register remains unchanged when "0" is written in this register.

Endpoint 0 Receive Byte Count Register (C9h, –)

D7	D6	D5	D4	D3	D2	D1	D0
RFU	EP0 Byte Count (R)						

Endpoint 1 Receive Byte Count Register (CAh, –)

D7	D6	D5	D4	D3	D2	D1	D0
RFU	EP1 Byte Count (R)						

Endpoint 2 Receive Byte Count Register (CBh, –)

D7	D6	D5	D4	D3	D2	D1	D0
RFU	EP2 Byte Count (R)						

Flash Transmit FIFO (–, 4Eh)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0				0

In case EP1 is set as a transmission endpoint, when "1" is written in this bit, the FIFO at EP1 is cleared and Packet Ready at EP1 is reset by the WRITE pulse.

In case EP2 is set as a transmission endpoint, when "1" is written in this bit, the FIFO at EP2 is cleared and Packet Ready at EP2 is reset by the WRITE pulse.

In case EP3 is set as a transmission endpoint, when "1" is written in this bit, the FIFO at EP3 is cleared and Packet Ready at EP3 is reset by the WRITE pulse.

Note: Please clear all FIFOs at the same time, otherwise some of them may not be cleared.

System Control (–, 4Fh)

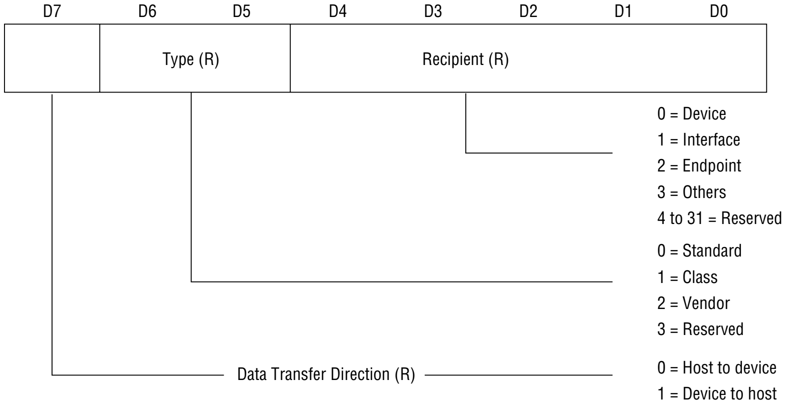
D7	D6	D5	D4	D3	D2	D1	D0
				0	0	0	

When "1" is written in this bit, the ML60851A is reset by the WRITE pulse.

Oscillation Stop Command

Oscillation Stop Command: Writing 1010b to D7 to D4, (writing A0h into this register) causes the oscillator circuit of the ML60851A to be deactivated and go into the standby mode.
When oscillation is stopped, reading and writing into the register is possible but reading and writing into FIFO is not possible. Asserting the $\overline{\text{RESET}}$ pin restarts oscillation.

bmRequestType Setup Register (D0h, –)



bRequest Setup Register (D1h, –)

D7	D6	D5	D4	D3	D2	D1	D0
Specific Request (R)							

- wValueLSB Setup Register (D2h, –)
  D7:D0 = LSB of Word Size Field (R)

- wValueMSB Setup Register (D3h, –)
  D7:D0 = MSB of Word Size Field (R)

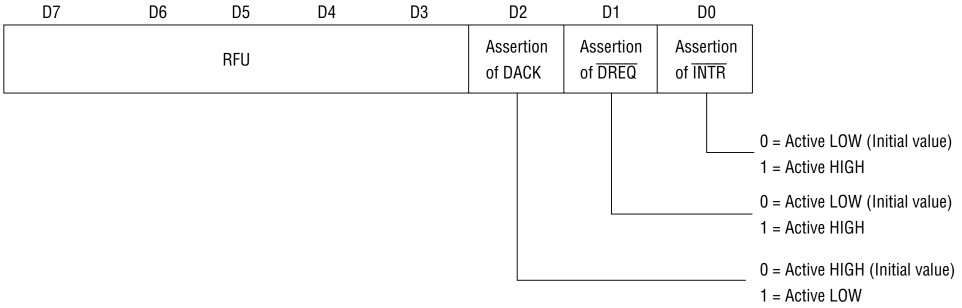
- wIndexLSB Setup Register (D4h, –)
  D7:D0 = LSB of Word Size Field (R)

- wIndexMSB Setup Register (D5h, –)
  D7:D0 = MSB of Word Size Field (R)

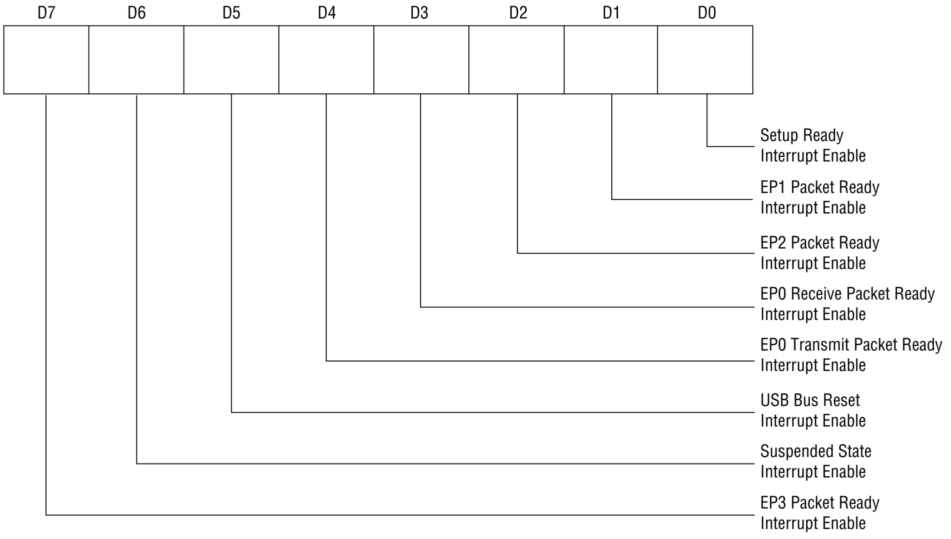
- wLengthLSB Setup Register (D6h, –)
  This field defines the length of data that is transferred in the second stage (data stage) of control transfer. (R)

- wLengthMSB Setup Register (D7h, –)
  This field defines the length of data that is transferred in the data stage of control transfer. (R)

Assertion Select Register (DAh, 5Ah) (R/W)

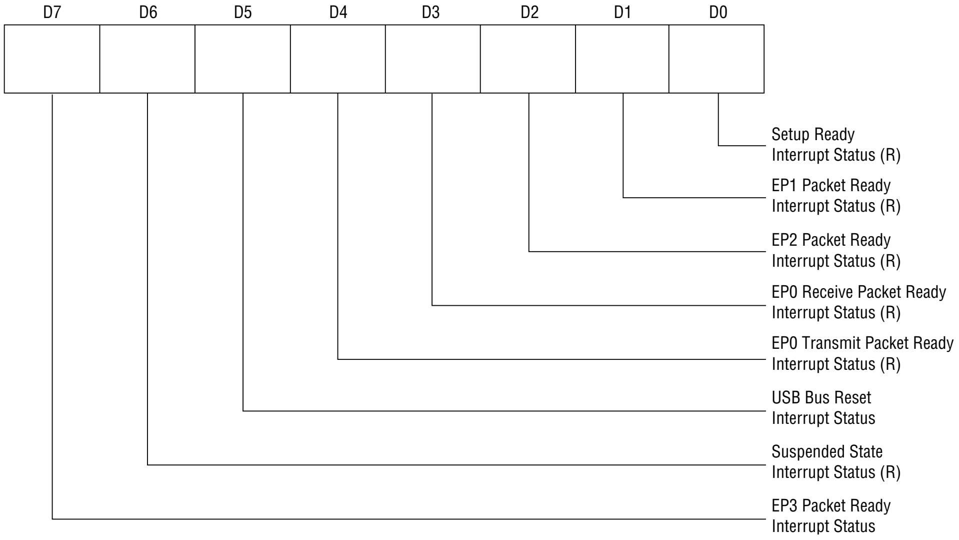

D7
D6
D5
D4
D3
D2
D1
D0
RFU
Assertion of DACK
Assertion of $\overline{\text{DREQ}}$
Assertion of $\overline{\text{INTR}}$
0 = Active LOW (Initial value)
1 = Active HIGH
0 = Active LOW (Initial value)
1 = Active HIGH
0 = Active HIGH (Initial value)
1 = Active LOW

Interrupt Enable Register (DBh, 5Bh) (R/W)


D7
D6
D5
D4
D3
D2
D1
D0
Setup Ready Interrupt Enable
EP1 Packet Ready Interrupt Enable
EP2 Packet Ready Interrupt Enable
EP0 Receive Packet Ready Interrupt Enable
EP0 Transmit Packet Ready Interrupt Enable
USB Bus Reset Interrupt Enable
Suspended State Interrupt Enable
EP3 Packet Ready Interrupt Enable

Initial value of D0 is 1.
Initial values of D1 to D7 are 0.

Interrupt Status Register (DCh, 5Ch) (R)


D7
D6
D5
D4
D3
D2
D1
D0
Setup Ready Interrupt Status (R)
EP1 Packet Ready Interrupt Status (R)
EP2 Packet Ready Interrupt Status (R)
EP0 Receive Packet Ready Interrupt Status (R)
EP0 Transmit Packet Ready Interrupt Status (R)
USB Bus Reset Interrupt Status
Suspended State Interrupt Status (R)
EP3 Packet Ready Interrupt Status

Setup Ready Interrupt Status: Equivalent to Setup Ready at (F3h) described later when the corresponding Interrupt Enable bit is asserted.

EP1 Packet Ready Interrupt Status: Equivalent to EP1 Receive Packet Ready (the complement of EP1 Transmit Packet Ready when EP1 is set for transmitter) at (C8h) described before when the corresponding Interrupt Enable bit is asserted.

EP2 Packet Ready Interrupt Status: Equivalent to EP2 Receive Packet Ready (the complement of EP2 Transmit Packet Ready when EP2 is set for transmitter) at (C8h) described before when the corresponding Interrupt Enable bit is asserted.

EP0 Receive Packet Ready Interrupt Status: Equivalent to EP0 Receive Packet Ready at (C8h) described before when the corresponding Interrupt Enable bit is asserted.

EP0 Transmit Packet Ready Interrupt Status: Equivalent to the complement of EP0 Transmit Packet Ready at (C8h) described before when the corresponding Interrupt Enable bit is asserted.

USB Bus Reset Interrupt Status: This bit is set to "1" at USB bus reset when the D5 bit of the interrupt enable register (DBh) is "1". To return this bit back to "0", "1" should be written to the D5 bit of the device states register.

Suspended State Interrupt Status: Equivalent to Suspended State Register at (C1h) described before when the corresponding Interrupt Enable bit is asserted.

EP3 Packet Ready Interrupt Status: When the D7 bit of the interrupt enable register (DBh) is "1", the complement of the D7 bit of the endpoint packet ready register (C8h) is being copied.

DMA Control Register (DDh, 5Dh) (R/W)

D7	D6	D5	D4	D3	D2	D1	D0
RFU			Transfer Mode	Transfer Size	Byte Count	Address Mode	DMA Enable

D0:
0 = Disables DMA Transfer (Initial value)
1 = Enables DMA Transfer for EP1

D1:
0 = Single Address Mode (Initial value)
1 = Dual Address Mode

D2:
0 = (Initial value)
1 = Inserts EP1 receive byte count into the top byte or top word of the transfer data. (Note 1)

D3:
0 = Byte (8 bits) (Initial value)
1 = Word (16 bits) (Note 2)

D4:
0 = Single Transfer Mode (Initial value)
1 = Demand Transfer Mode

(Note 1) When 16-bit mode is set, the upper byte of the top word is 00h.
(Note 2) When 16-bit mode is set and the packet size is an odd-number byte, the upper byte of the last word is 00h.

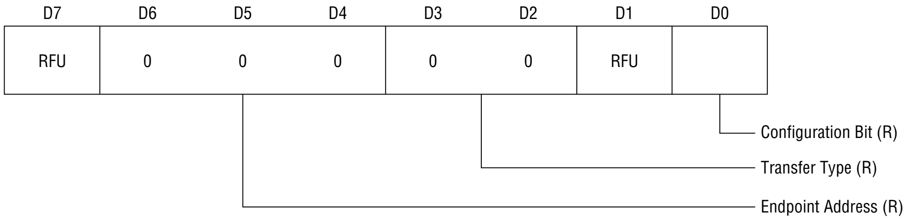
DMA Interval Register (DEh, 5Eh) (R/W)

D7	D6	D5	D4	D3	D2	D1	D0

This register specifies a DMA transfer interval between de-assertion and re-assertion of DREQ in Single Transfer mode. The interval is specified between 0 and 255 (bit times). The initial value is 0.

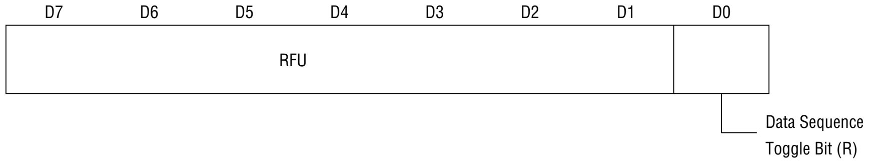
1-bit time = 1/12 MHz (= 84 ns)

Endpoint 0 Receive Control Register (E0h, –)

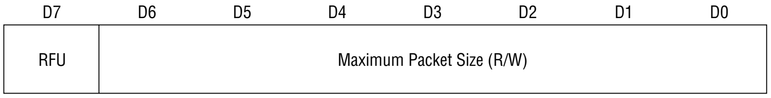


Configuration Bit: Only when this bit is asserted ("1"), a packet transmitted from a host computer to this EP is received. The packet is ignored when this bit is deasserted ("0").
This bit is deasserted by system reset and is asserted by USB reset (both D+ and D- are 0s for more than 2.5 µs).

Endpoint 0 Receive General Register (E1h, –)

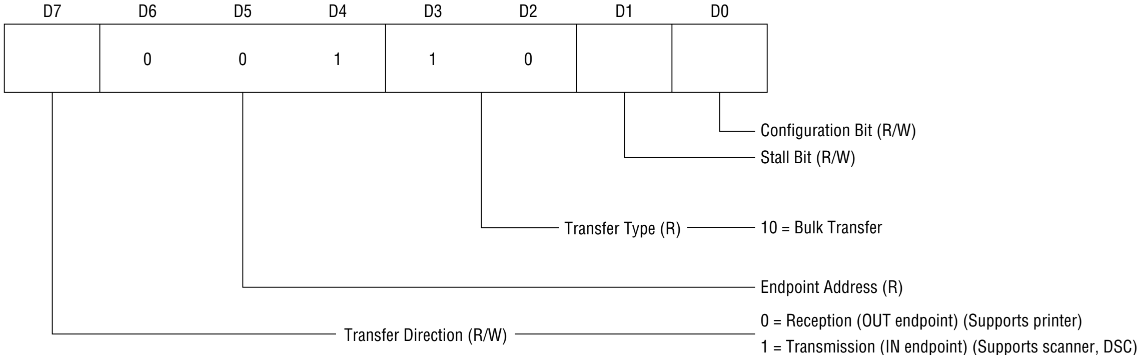


Endpoint 0 Receive Payload Register (E2h, 62h)



Endpoint 1 Control Register (E4h, 64h)

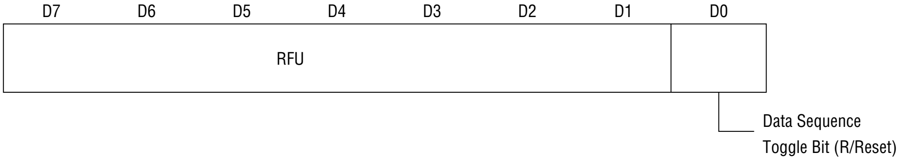
Register to set the attribute of EP1.
To use EP1, the local MCU writes EP1's attribute in this register by the request from the host computer.



Configuration Bit: Only when this bit is asserted ("1"), a packet transmitted from the host computer to this EP is received. The packet is ignored when this bit is deasserted ("0").
Whether or not this EP is configured can be known by referencing this bit.

Stall Bit: When this bit is asserted ("1"), a stall handshake for a packet transmitted from the host computer to this EP is automatically returned to the host computer.

Endpoint 1 General Register (E5h, 65h)



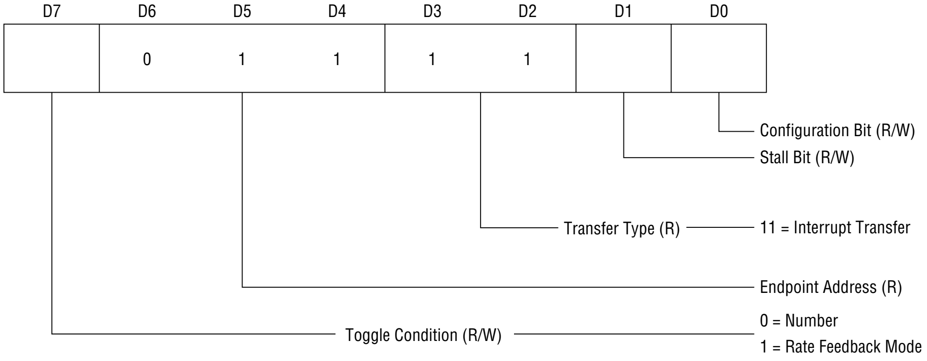
Data Sequence Toggle Bit: When initializing EP, PID of DATA0 is specified after resetting the Data Packet Toggle bit by writing "1" to this bit (this bit goes to "0").

Endpoint 1 Payload Register (E6h, 66h)

D7	D6	D5	D4	D3	D2	D1	D0
RFU	Maximum packet size (R/W)						

Endpoint 3 Control Register (F8h, 78h)

Register to set the attribute of EP3.
To use EP3, the local MCU writes EP3's attribute in this register by the request from the host computer.

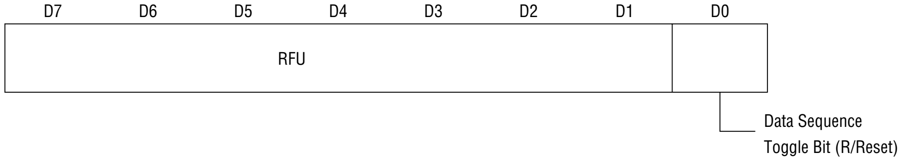


Configuration Bit: Only when this bit is asserted ("1"), a packet transmitted from the host computer to this EP is received. The packet is ignored when this bit is deasserted ("0").
Whether or not this EP is configured can be known by referencing this bit.

Stall Bit: When this bit is asserted ("1"), a stall handshake for a packet transmitted from the host computer to this EP is automatically returned to the host computer.

Toggle Condition Bit: When this bit is "0", DATA0 and DATA1 are toggled each time ACK is received form the host computer by the EP3. Setting this bit to "1" causes the ML60851A to go into the rate feedback mode, in which case DATA0 and DATA1 are toggled each time the packet ready is asserted by the local MCU.

Endpoint 3 General Register (F9h, 79h)

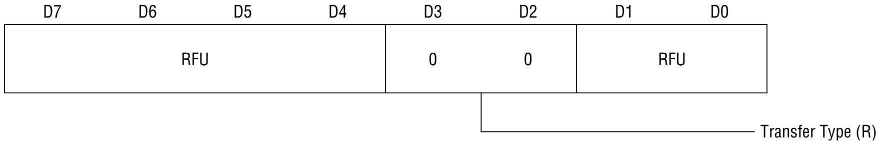


Data Sequence Toggle Bit: When initializing EP, PID of DATA0 is specified after resetting the Data Packet Toggle bit by writing "1" to this bit (this bit goes to "0").

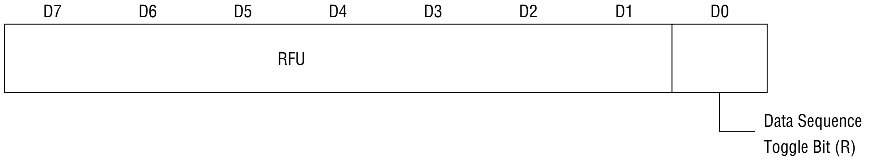
Endpoint 3 Payload Register (FAh, 7Ah)

D7	D6	D5	D4	D3	D2	D1	D0
RFU	Maximum packet size (R/W)						

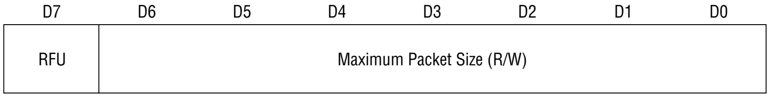
Endpoint 0 Transmit Control Register (F0h, –)



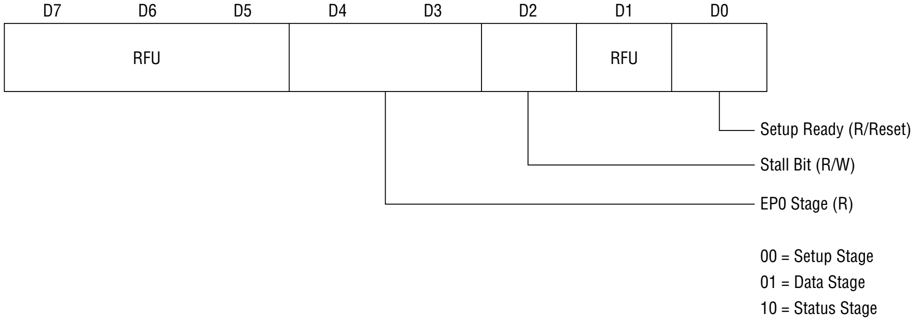
Endpoint 0 Transmit General Register (F1h, –)



Endpoint 0 Transmit Payload Register (F2h, 72h)



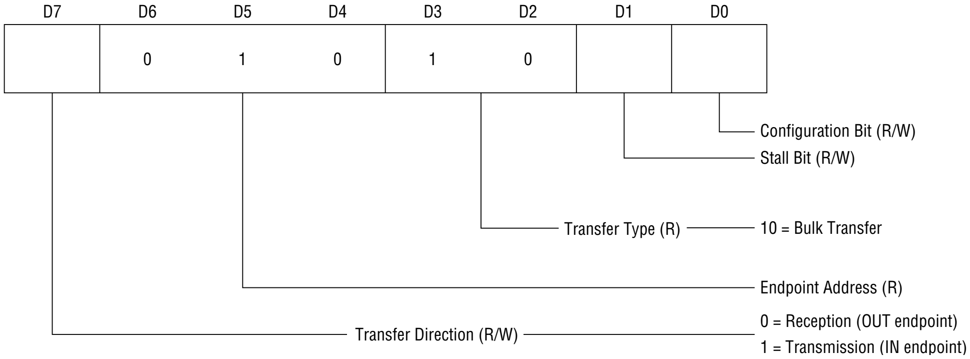
Endpoint 0 Transmit General Register (F3h, 73h)



Setup Ready: When a valid setup packet has arrived at an 8-byte setup register, this register is automatically set and the receive FIFO at endpoint 0 is locked. Writing "1" in this register resets Setup Ready. When the data stage of Control Write transaction follows, Packet Ready at endpoint 0 is also reset. Therefore, the endpoint 0 receive FIFO is unlocked and ready to receive the packets in the data stage.

The value of this register remains unchanged when "0" is written in this register.

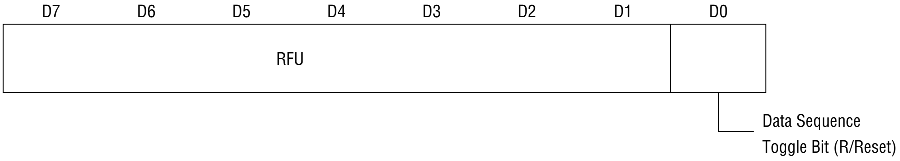
Endpoint 2 Control Register (F4h, 74h)



Configuration Bit: Only when this bit is asserted ("1"), a packet transmitted from the host computer to this EP is received. The packet is ignored when this bit is deasserted ("0").
Whether or not this EP is configured can be known by referencing this bit.

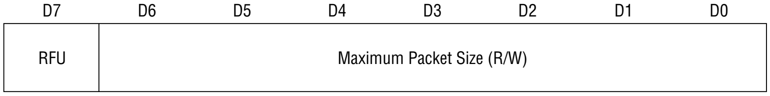
Stall Bit: When this bit is asserted ("1"), a stall handshake for a packet transmitted from the host computer to this EP is automatically returned to the host computer.

Endpoint 2 General Register (F5h, 75h)



Data Sequence Toggle Bit: When initializing EP, PID of DATA0 is specified after resetting the Data Packet Toggle bit by writing "1" to this bit (this bit goes to "0").

Endpoint 2 Payload Register (F6h, 76h)



Endpoint 0 Receive FIFO Data (40h, –)

<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="8">Endpoint 0 Receive FIFO Data (R)</td></tr>
</table>

Area to store data to be transmitted from the host computer to this device in the data stage of Control Write transfer.

Endpoint 1 Receive FIFO Data (41h, –)

<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="8">Endpoint 1 Receive FIFO Data (R)</td></tr>
</table>

Area to store data to be transmitted from the host computer to EP1 of this device in Bulk Out transfer. This register is valid only when EP1 is set for the OUT endpoint.

Endpoint 2 Receive FIFO Data (42h, –)

<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="8">Endpoint 2 Receive FIFO Data (R)</td></tr>
</table>

Area to store data to be transmitted from the host computer to EP2 of this device in Bulk Out transfer. This register is valid only when EP2 is set for the OUT endpoint.

Endpoint 0 Transmit FIFO Data (–, C0h)

D7	D6	D5	D4	D3	D2	D1	D0
Endpoint 0 Transmit FIFO Data (W)							

Area to store data to be transmitted from this device to the host computer in the data stage of Control Read transter.

Endpoint 1 Transmit FIFO Data (–, C1h)

D7	D6	D5	D4	D3	D2	D1	D0
Endpoint 1 Transmit FIFO Data (W)							

Area to store data to be transmitted from EP1 of this device to the host computer in Bulk In transfer. This register is valid only when EP1 is set for the IN endpoint.

Endpoint 2 Transmit FIFO Data (–, C2h)

D7	D6	D5	D4	D3	D2	D1	D0
Endpoint 2 Transmit FIFO Data (W)							

Area to store data to be transmitted from EP2 of this device to the host computer in Bulk In transfer. This register is valid only when EP2 is set for the IN endpoint.

Endpoint 3 Transmit FIFO Data (–, C3h)

D7	D6	D5	D4	D3	D2	D1	D0
Endpoint 3 Transmit FIFO Data (W)							

Area to store data to be transmitted from EP3 of this device to the host computer in Bulk In transfer. This register is valid only when EP3 is set for the IN endpoint.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply 3	V_{CC3}	—	–0.3 to +4.6	V
Power Supply 5	V_{CC5}	—	–0.5 to +6.5	V
Input Voltage	V_I	—	–0.3 to V_{CC5} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply 3	V_{CC3}	—	3.0 to 3.6	V
Power Supply 5	V_{CC5}	—	3.0 to 5.5	V
Operating Temperature	Ta	—	0 to 70	°C
Oscillation Frequency	F_{OSC}	—	48	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{CC5} = V_{CC3} = 3.0 to 3.6 V, V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
High-level Input Voltage	V_{IH}	—	2.0	—	V_{CC5} + 0.3	V	Note 1
Low-level Input Voltage	V_{IL}	—	–0.3	—	+0.8	V	
High-level Input Voltage	V_{IH}	—	$V_{CC3} \times 0.8$	—	V_{CC3} + 0.3	V	XIN
Low-level Input Voltage	V_{IL}	—	–0.3	—	$V_{CC3} \times 0.2$	V	
Schmitt Trigger Input Voltage	V_{t+}	—	—	1.6	2.0	V	$\overline{RESET}$
	V_{t-}	—	0.8	1.2	—	V	
	ΔV_t	$(V_{t+}) - (V_{t-})$	0.1	0.4	—	V	
High-level Output Voltage	V_{OH}	I_{OH} = –100 μA	V_{CC5} – 0.2	—	—	V	D15:D8 AD7:AD0 $\overline{INTR}$, $\overline{DREQ}$
		I_{OH} = –4 mA	2.4	—	—	V	
Low-level Output Voltage	V_{OL}	I_{OL} = 100 μA	—	—	0.2	V	
		I_{OL} = 4 mA	—	—	0.4	V	
High-level Input Current	I_{IH}	V_{IH} = V_{CC5}	—	0.01	1	μA	Note 2
Low-level Input Current	I_{IL}	V_{IL} = V_{SS}	–1	–0.01	—	μA	
3-state Output Leakage Current	I_{OZH}	V_{OH} = V_{CC5}	—	0.01	1	μA	D15:D8 AD7:AD0
	I_{OZL}	V_{OL} = V_{SS}	–1	–0.01	—	μA	
Power Supply Current (Operating)	I_{CC3}	—	—	—	50	mA	V_{CC3}
	I_{CC5}	—	—	—	5	mA	V_{CC5}
Power Supply Current (Standby)	I_{CCS3}	Note 3	—	—	50	μA	V_{CC3}
	I_{CCS5}	Note 3	—	—	50	μA	V_{CC5}

Notes: 1. Applied to D15:D8, AD7:AD0, A7:A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DACK, ALE, and ADSEL.
2. Applied to XIN, A7:A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DACK, ALE, and ADSEL. V_{IH} = V_{CC3} for only XIN.
3. The XIN pin is fixed to High level or Low level in the suspend state. All the output pins are open.

DC Characteristics (2)

(V_{CC5} = 4.5 to 5.5 V, V_{CC3} = 3.0 to 3.6 V, V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
High-level Input Voltage	V_{IH}	—	2.2	—	$V_{CC5} + 0.5$	V	Note 1
Low-level Input Voltage	V_{IL}	—	–0.5	—	+0.8	V	
Schmitt Trigger Input Voltage	V_{t+}	—	—	1.7	2.2	V	$\overline{\text{RESET}}$
	V_{t-}	—	0.8	1.4	—	V	
	ΔV_t	$(V_{t+}) - (V_{t-})$	0.2	0.3	—	V	
High-level Output Voltage	V_{OH}	$I_{OH} = -100\ \mu A$	$V_{CC5} - 0.2$	—	—	V	D15:D8 AD7:AD0 $\overline{\text{INTR}}$, $\overline{\text{DREQ}}$
		$I_{OH} = -8$ mA	3.7	—	—	V	
Low-level Output Voltage	V_{OL}	$I_{OL} = 100\ \mu A$	—	—	0.2	V	
		$I_{OL} = 8$ mA	—	—	0.4	V	
High-level Input Current	I_{IH}	$V_{IH} = V_{CC5}$	—	0.01	10	µA	Note 2
Low-level Input Current	I_{IL}	$V_{IL} = V_{SS}$	–10	–0.01	—	µA	
3-state Output Leakage Current	I_{OZH}	$V_{OH} = V_{CC5}$	—	0.01	10	µA	D15:D8
	I_{OZL}	$V_{OL} = V_{SS}$	–10	–0.01	—	µA	AD7:AD0
Power Supply Current (Operating)	I_{CC3}	—	—	—	50	mA	V_{CC3}
	I_{CC5}	—	—	—	5	mA	V_{CC5}
Power Supply Current (Standby)	I_{CCS3}	Note 3	—	—	50	µA	V_{CC3}
	I_{CCS5}	Note 3	—	—	50	µA	V_{CC5}

Notes:
1. Applied to D15:D8, AD7:AD0, A7:A0, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DACK, ALE, and ADSEL. The DC characteristics (1) applies to XIN.
2. Applied to A7:A0, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DACK, ALE, and ADSEL. The DC characteristics (1) applies to XIN.
3. The XIN pin is fixed to High level or Low level in the suspend state. All the output pins are open.

DC Characteristics (3) USB Port

(V_{CC3} = 3.0 to 3.6 V, V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Differential Input Sensitivity	V_{DI}	(D+) – (D–)	0.2			V	D+, D–
Differential Common Mode Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V	
Single Ended Receiver Threshold	V_{SE}		0.8		2.0	V	
High-level Output Voltage	V_{OH}	RL of 15 kΩ to V_{SS}	2.8		3.6	V	
Low-level Output Voltage	V_{OL}	RL of 1.5 kΩ to 3.6 V			0.3	V	
Output Leakage Current	I_{LO}	0 V < V_{IN} < 3.3 V	–10		+10	μA	

AC Characteristics USB Port

(V_{CC3} = 3.0 to 3.6 V, V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition (Notes 1. and 2.)	Min.	Typ.	Max.	Unit	Applicable pin
Rise Transition Time	t_R	CL = 50 pF	4		25	ns	D+, D–
Fall Transition Time	t_F	CL = 50 pF	4		25	ns	
Rise/Fall Time Matching	t_{RFM}	(t_R/t_F)	90		140	%	
Output Signal Crossover Voltage	V_{CRS}		1.2		2	V	
Driver Output Resistance	Z_{DRV}	Steady State Driver	28		43	Ω	
Data Rate	t_{DRATE}	Ava. Bit Rate (12 Mb/s ±0.25%)	11.97		12.03	Mbs	

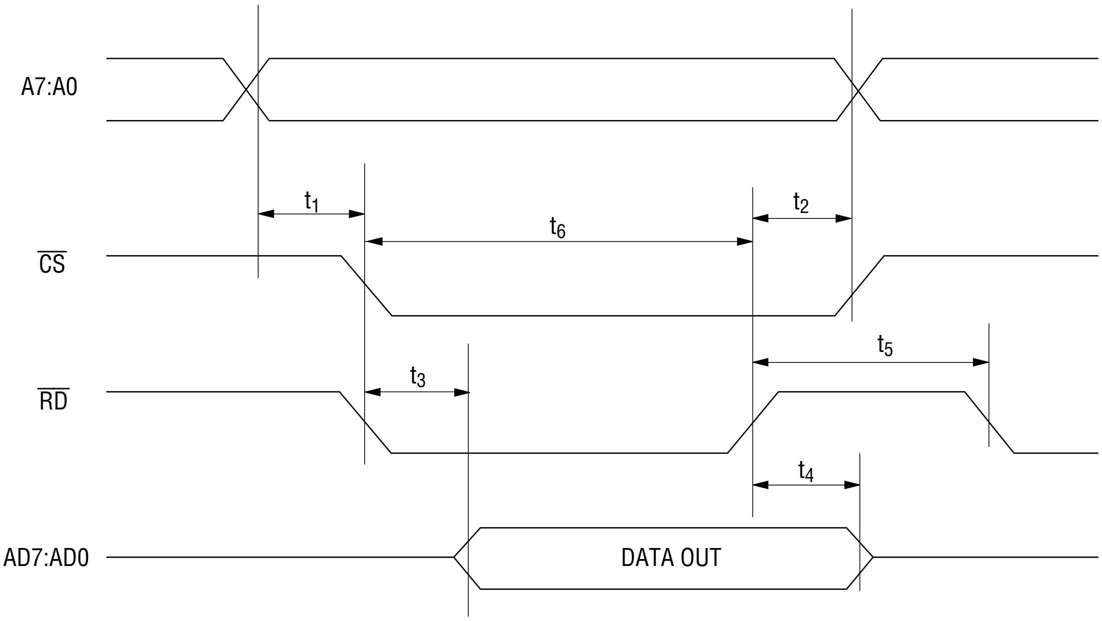
Notes: 1. 1.5 kΩ pull-up to 2.8 V on the D+ data line.
2. Measured from 10% to 90% of the data signal.

TIMING DIAGRAM

READ Timing (1)
(Address Separate ADSEL = 0)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Address Setup Time ($\overline{RD}$)	t_1 ($\overline{RD}$)		21	—	ns	5
Address Setup Time ($\overline{CS}$)	t_1 ($\overline{CS}$)		10	—	ns	5
Address ($\overline{CS}$) Hold Time	t_2		0	—	ns	2
Read Data Delay Time	t_3	Load 20 pF	—	25	ns	1
Read Data Hold Time	t_4		0	—	ns	
Recovery Time	t_5	FIFO READ	63	—	ns	3
FIFO Access Time	t_6	FIFO READ	42	—	ns	4

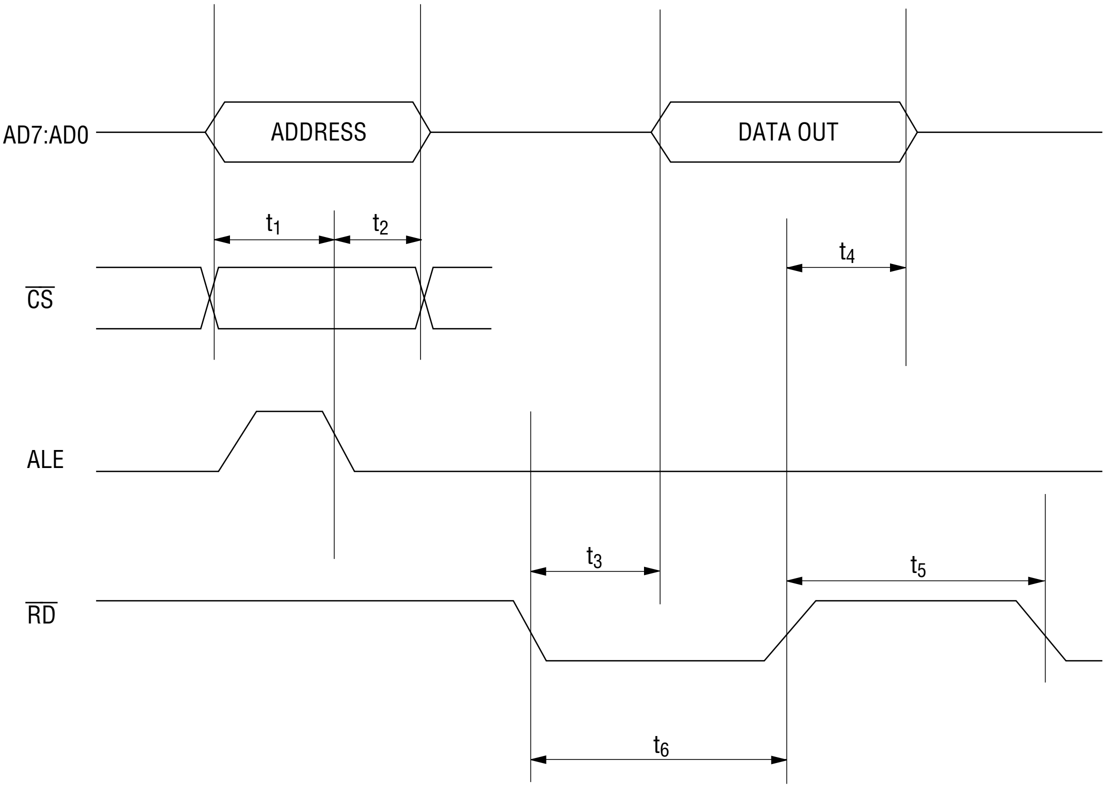
Notes:
1. t_1 and t_3 are defined depending upon $\overline{CS}$ or $\overline{RD}$ which becomes active last.
2. t_2 is defined depending upon $\overline{CS}$ or $\overline{RD}$ which becomes active first.
3. 3-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
4. 2-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
5. Either of them should be met.



READ Timing (2)
(Address/Data Multiplex ADSEL = 1)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Address ($\overline{CS}$) Setup Time	t_1		10	—	ns	
Address ($\overline{CS}$) Hold Time	t_2		0	—	ns	
Read Data Delay Time	t_3	Load 20 pF	—	25	ns	
Read Data Hold Time	t_4		0	—	ns	
Recovery Time	t_5	FIFO READ	63	—	ns	1
FIFO Access Time	t_6	FIFO READ	42	—	ns	2

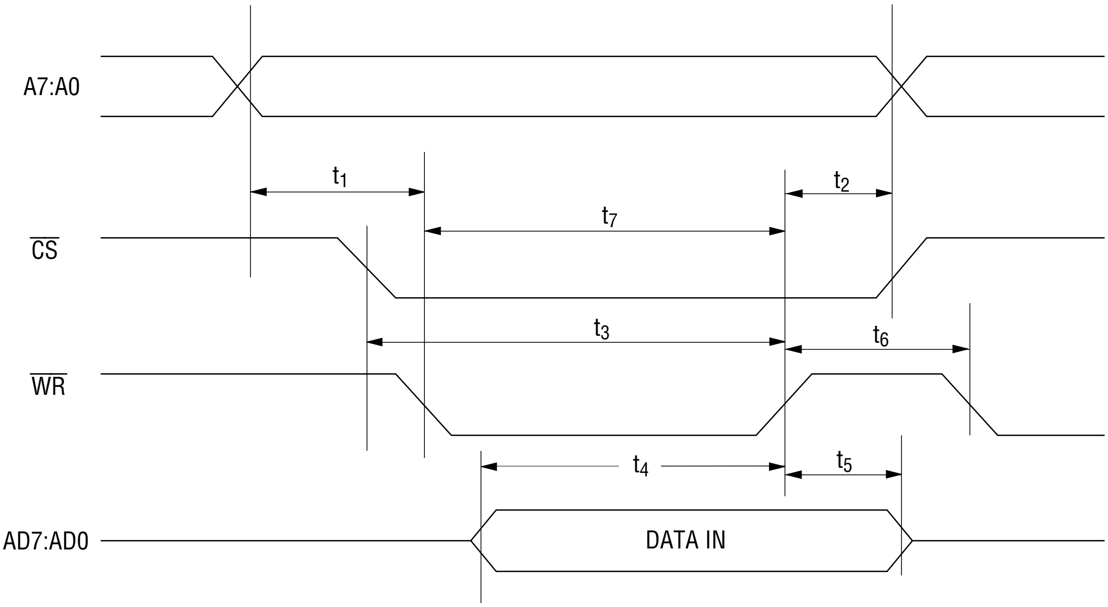
Notes: 1. 3-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
2. 2-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.



WRITE Timing (1)
(Address Separate ADSEL = 0)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Address Setup Time ($\overline{WR}$)	t_1 ($\overline{WR}$)		21	—	ns	4
Address Setup Time ($\overline{CS}$)	t_1 ($\overline{CS}$)		10	—	ns	4
Address ($\overline{CS}$) Hold Time	t_2		0	—	ns	
$\overline{CS}$ Setup Time	t_3		10	—	ns	
Write Data Setup Time	t_4		30	—	ns	
Write Data Hold Time	t_5		5	—	ns	
Recovery Time	t_6	FIFO WRITE	63	—	ns	2
FIFO Access Time	t_7	FIFO WRITE	42	—	ns	3

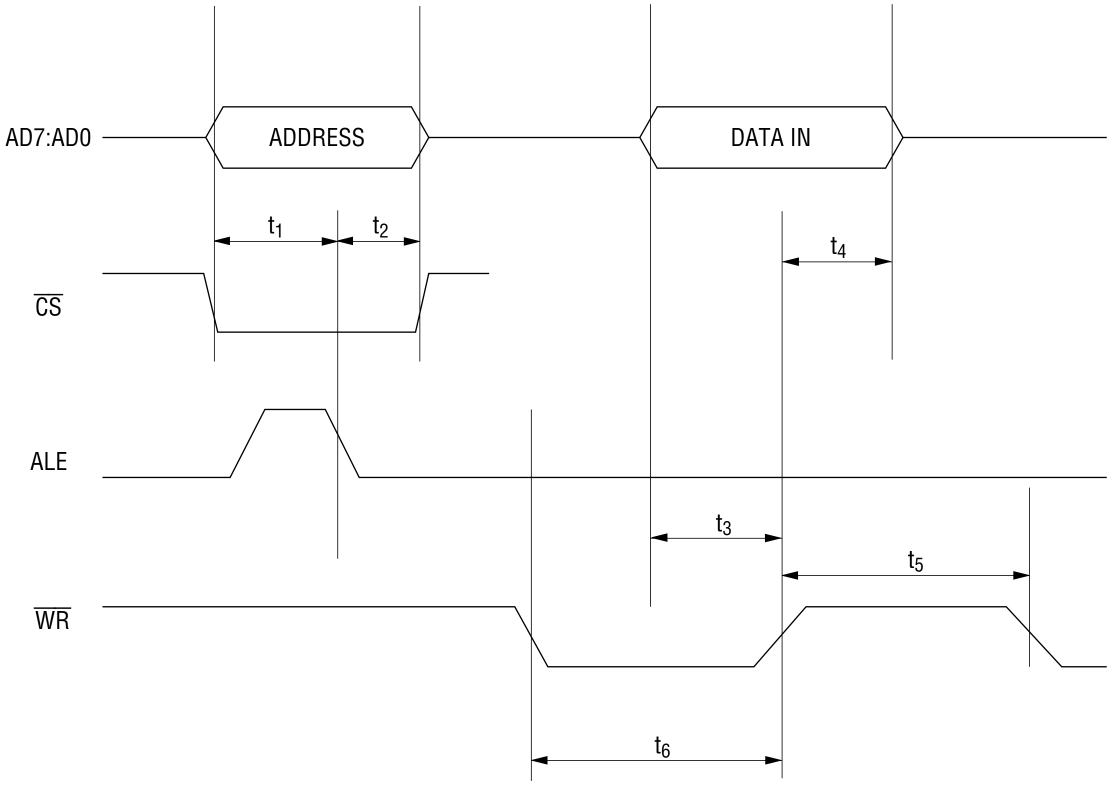
Notes:
1. t_1 is defined depending upon $\overline{CS}$ or $\overline{WR}$ which becomes active last.
2. 3-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
3. 2-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
4. Either of them should be met.



WRITE Timing (2)
(Address/Data Multiplex ADSEL = 1)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Address ($\overline{CS}$) Setup Time	t_1		10	—	ns	
Address ($\overline{CS}$) Hold Time	t_2		0	—	ns	
Write Data Setup Time	t_3		30	—	ns	
Write Data Hold Time	t_4		5	—	ns	
Recovery Time	t_5	FIFO WRITE	63	—	ns	1
FIFO Access Time	t_6	FIFO WRITE	42	—	ns	2

Notes:
1. 3-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
2. 2-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.

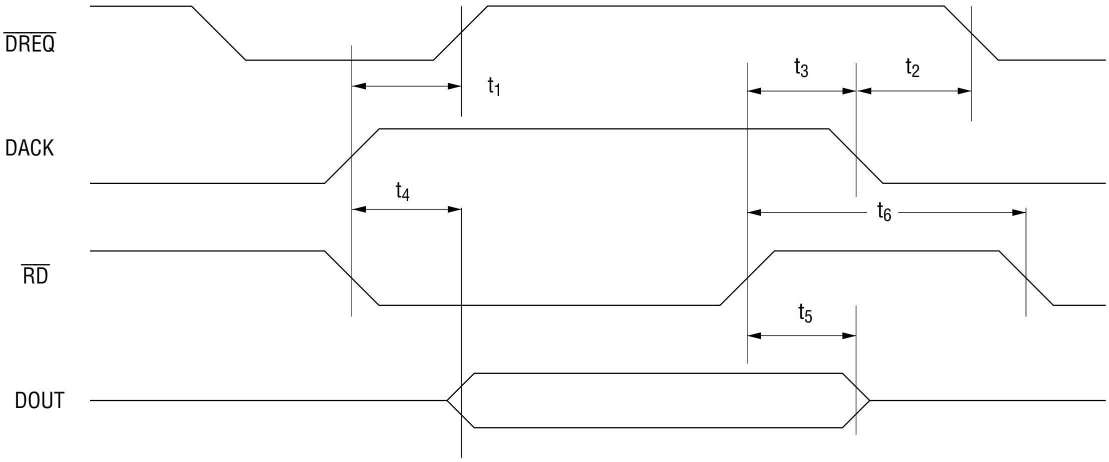


DMA Transfer Timing (1)

ML60851A to Memory (Single Transfer, Single Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
$\overline{\text{DREQ}}$ Enable Time	t_2		—	63	ns	
DACK Hold Time	t_3		0	—	ns	
Read Data Delay Time	t_4	Load 20 pF	—	25	ns	1
Data Hold Time	t_5		0	—	ns	
Recovery Time	t_6	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Single Address mode, $\overline{\text{CS}}$ and A7:A0 are ignored.
t_4 is defined depending on DACK or $\overline{\text{RD}}$ which becomes active last.
2. 3-clock time of oscillation clock (clock period: 21 ns).
3. 5-clock time of oscillation clock (clock period: 21 ns).

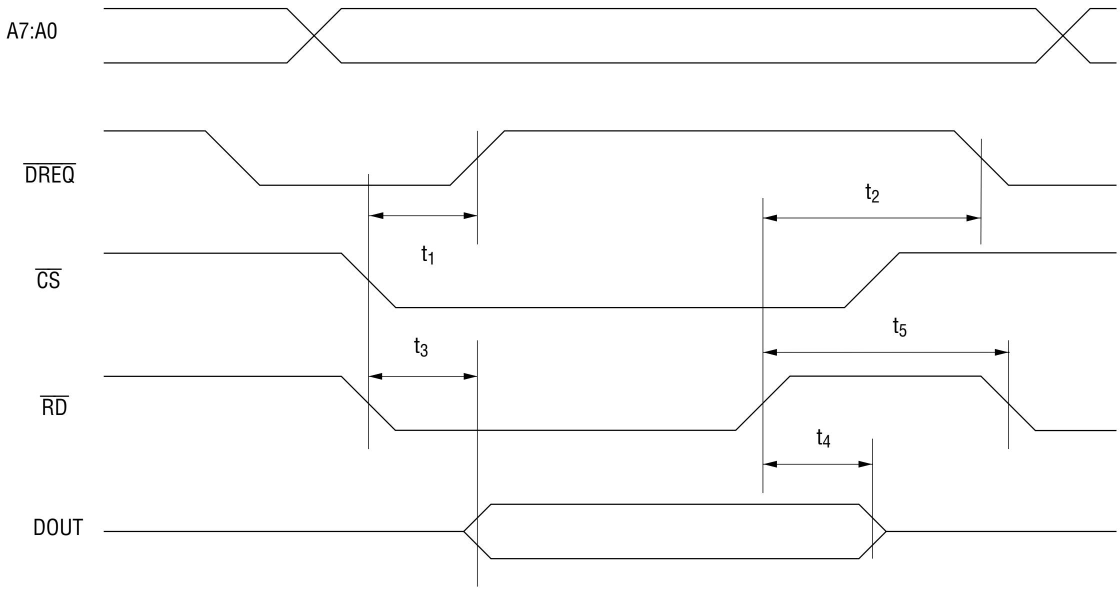


DMA Transfer Timing (2)

ML60851A to Memory (Single Transfer, Dual Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
$\overline{\text{DREQ}}$ Enable Time	t_2		—	63	ns	
Read Data Delay Time	t_3	Load 20 pF	—	25	ns	1
Data Hold Time	t_4		0	—	ns	
Recovery Time	t_5	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Dual Address mode, the DACK is ignored.
t_3 is defined depending on $\overline{\text{CS}}$ or $\overline{\text{RD}}$ which becomes active last.
A7:A0 specifies the FIFO address.
Refer to READ Timing (1) for Address Setup Time and Address Hold Time.
2. 3-clock time of oscillation clock (clock period: 21 ns).
3. 5-clock time of oscillation clock (clock period: 21 ns).

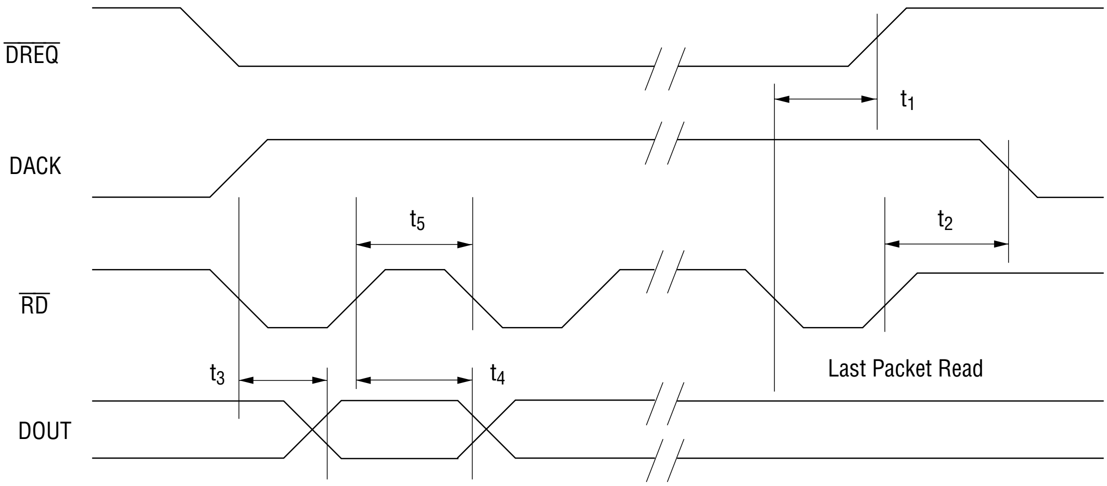


DMA Transfer Timing (3)

ML60851A to Memory (Demand Transfer, Single Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
DACK Hold Time	t_2		0	—	ns	
Read Data Delay Time	t_3	Load 20 pF	—	25	ns	1
Data Hold Time	t_4		0	—	ns	
Recovery Time	t_5	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes:
1. When in Single Address mode, t_3 is defined depending on DACK or $\overline{\text{RD}}$ which becomes active last.
   A7:A0 and $\overline{\text{CS}}$ are ignored.
2. 3-clock time of oscillation clock (clock period: 21 ns).
3. 5-clock time of oscillation clock (clock period: 21 ns).

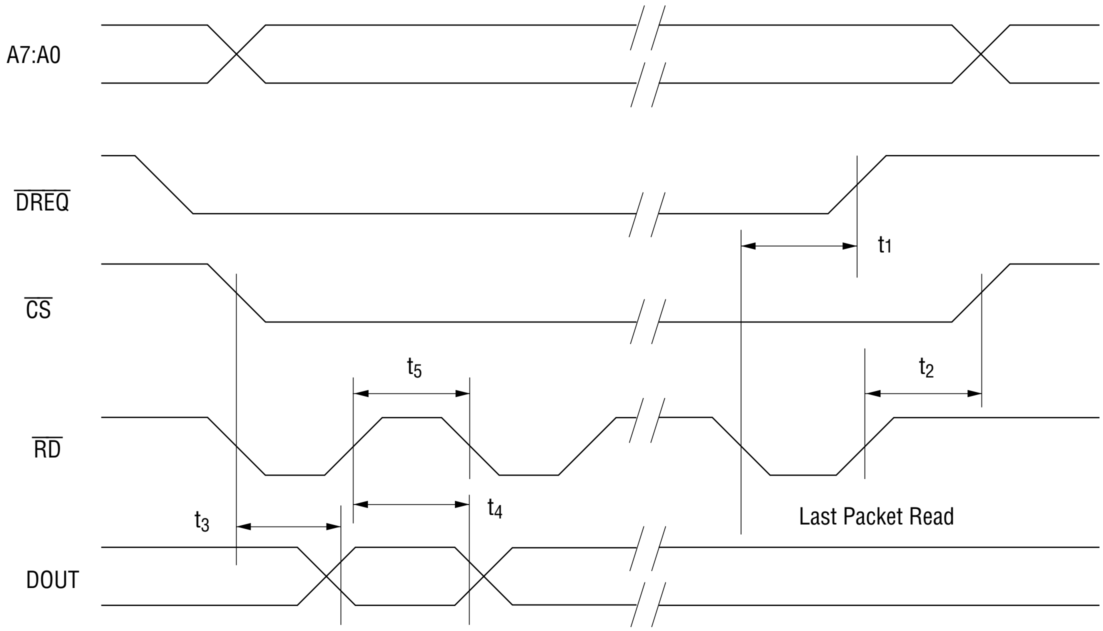


DMA Transfer Timing (4)

ML60851A to Memory (Demand Transfer, Dual Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
$\overline{\text{CS}}$ Hold Time	t_2		0	—	ns	
Read Data Delay Time	t_3	Load 20 pF	—	25	ns	1
Data Hold Time	t_4		0	—	ns	
Recovery Time	t_5	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes:
1. When in Dual Address mode, the DACK is ignored.
   t_3 is defined depending on $\overline{\text{CS}}$ or $\overline{\text{RD}}$ which becomes active last.
   A7:A0 specifies the FIFO address.
   Refer to READ Timing (1) for Address Setup Time and Address Hold Time.
2. 3-clock time of oscillation clock (clock period: 21 ns).
3. 5-clock time of oscillation clock (clock period: 21 ns).

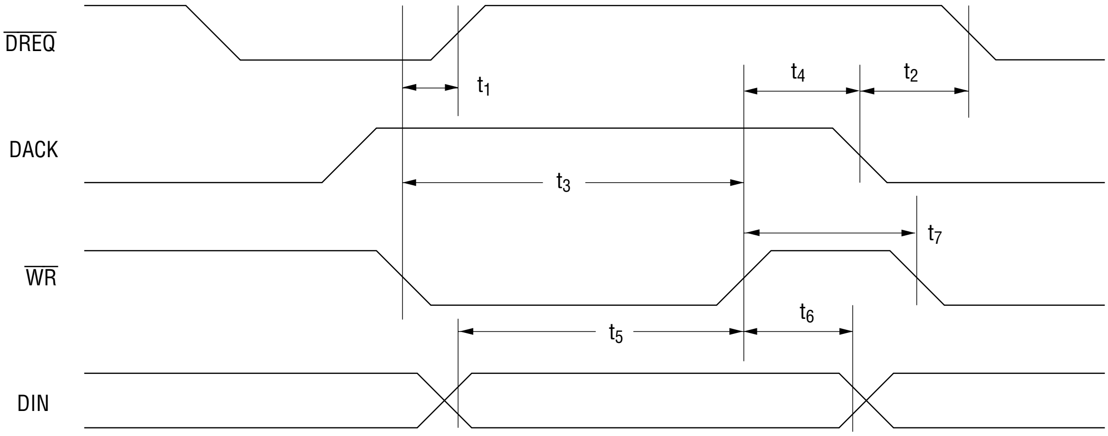


DMA Transfer Timing (5)

Memory to ML60851A (Single Transfer, Single Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
$\overline{\text{DREQ}}$ Enable Time	t_2		—	63	ns	
FIFO Access Time	t_3	FIFO WRITE	42	—	ns	1
DACK Hold Time	t_4		0	—	ns	
Write Data Setup Time	t_5		30	—	ns	
Write Data Hold Time	t_6		5	—	ns	
Recovery Time	t_7	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Single Address mode, $\overline{\text{CS}}$ and A7:A0 are ignored.
2. 3-clock time of oscillation clock (clock period: 21 ns).
3. 5-clock time of oscillation clock (clock period: 21 ns).

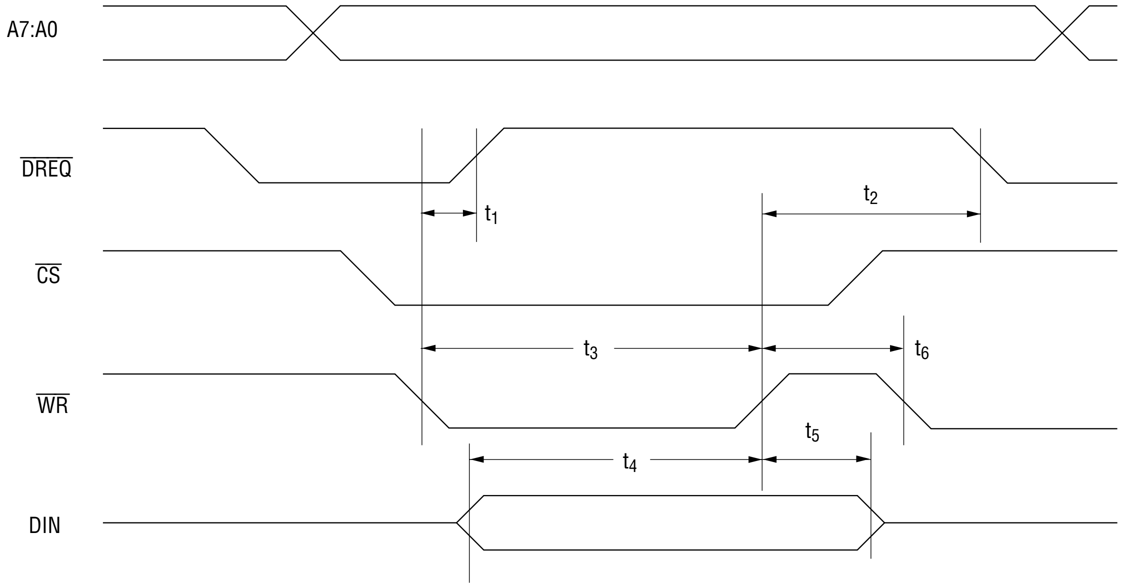


DMA Transfer Timing (6)

Memory to ML60851A (Single Transfer, Dual Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
$\overline{\text{DREQ}}$ Enable Time	t_2		—	63	ns	
FIFO Access Time	t_3	FIFO WRITE	42	—	ns	1
Write Data Setup Time	t_4		30	—	ns	
Write Data Hold Time	t_5		5	—	ns	
Recovery Time	t_6	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Dual Address mode, the DACK is ignored.
Refer to WRITE Timing (1) for Address Setup Time and Address Hold Time.
2. 3-clock time of oscillation clock (clock period: 21 ns).
3. 5-clock time of oscillation clock (clock period: 21 ns).

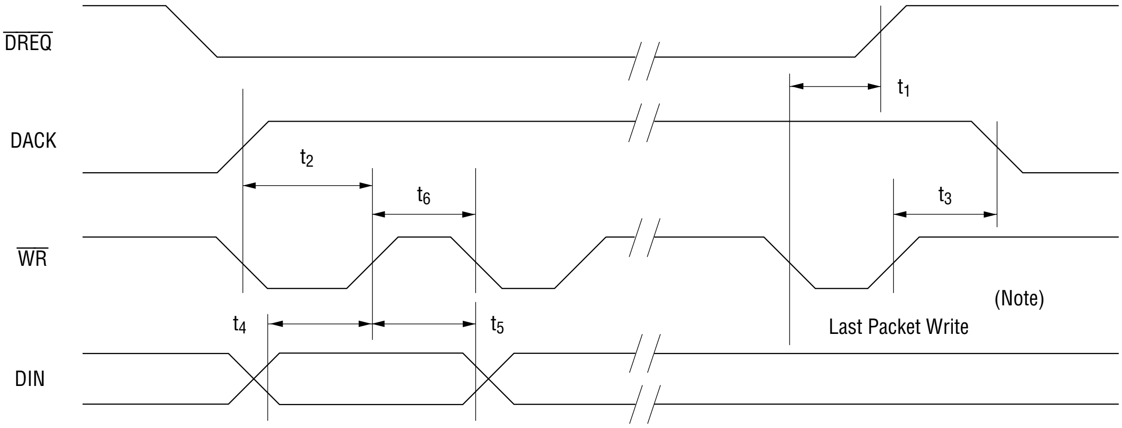


DMA Transfer Timing (7)

Memory to ML60851A (Demand Transfer, Single Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
FIFO Access Time	t_2	FIFO WRITE	42	—	ns	1
DACK Hold Time	t_3		0	—	ns	
Write Data Setup Time	t_4		30	—	ns	
Write Data Hold Time	t_5		5	—	ns	
Recovery Time	t_6	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Single Address mode, A7:A0 and $\overline{\text{CS}}$ and ignored.
2. 3-clock time of oscillation clock (clock period: 21 ns).
3. 5-clock time of oscillation clock (clock period: 21 ns).



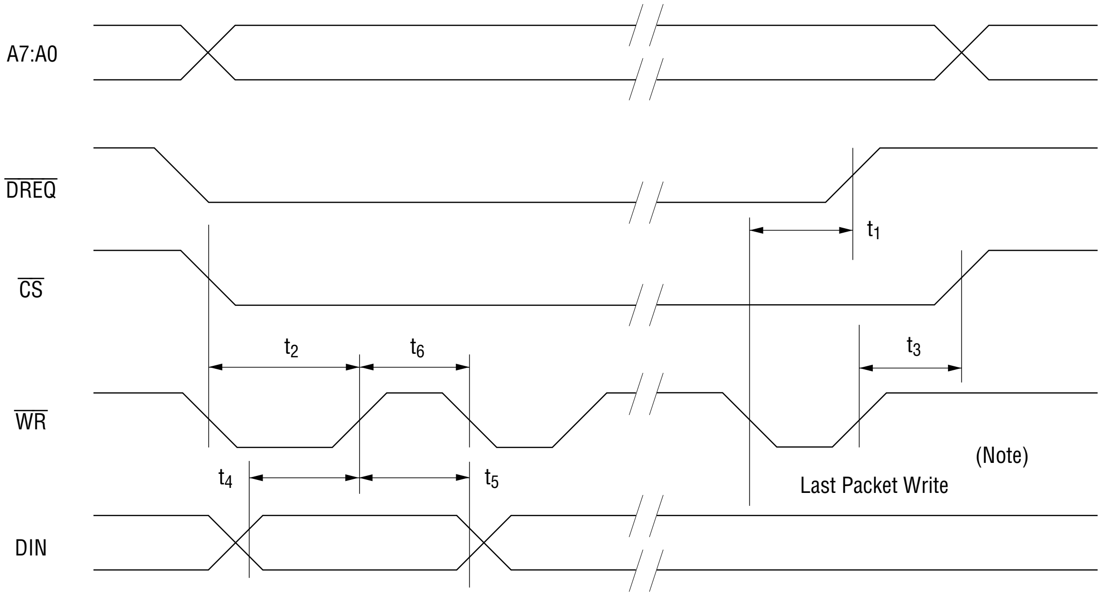
(Note) The last Write to reach the byte size (maximum packet size) specified by the EP1 Payload Register.
To terminate DMA transfer before reaching the maximum packet size, set EP1 Packet Ready by writing "1" to the EP1 Transmit Packet Ready bit.

DMA Transfer Timing (8)

Memory to ML60851A (Demand Transfer, Dual Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
FIFO Access Time	t_2	FIFO WRITE	42	—	ns	1
$\overline{\text{CS}}$ Hold Time	t_3		0	—	ns	
Write Data Setup Time	t_4		30	—	ns	
Write Data Hold Time	t_5		5	—	ns	
Recovery Time	t_6	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Dual Address mode, the DACK is ignored.
A7:A0 specifies the FIFO address.
Refer to WRITE Timing (1) for Address Setup Time and Address Hold Time.
2. 3-clock time of oscillation clock (clock period: 21 ns).
3. 5-clock time of oscillation clock (clock period: 21 ns).



(Note) Refer to the previous page.

FUNCTIONAL DESCRIPTIONS

Pin Functional Description

USB Interface

<table>
<tr><th>Signal</th><th>Type</th><th>Assertion</th><th>Description</th></tr>
<tr><td>D+</td><td>I/O</td><td>—</td><td>USB data (Plus). This signal and the D– signal are the transmitted or received data from/to USB Bus. The table below shows values and results for these signal.
<table>
<tr><th>D+</th><th>D–</th><th>Result</th></tr>
<tr><td>0</td><td>0</td><td>Single end 0</td></tr>
<tr><td>0</td><td>1</td><td>Differential "0"</td></tr>
<tr><td>1</td><td>0</td><td>Differential "1"</td></tr>
<tr><td>1</td><td>1</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>D–</td><td>I/O</td><td>—</td><td>USB Data (Minus). This signal and the D+ signal are the transmitted or received data from/to USB Bus. The table above shows values and results for these signals.</td></tr>
</table>

Crystal Oscillator Interface

Signal	Type	Assertion	Description
XIN	I	—	For internal oscillation, connect a crystal to XIN and XOUT. For external oscillation, supply an external 48 MHz clock signal to XIN. Set XOUT to be open.
XOUT	O	—	

Application Interface

Signal	Type	Assertion	Description
D15:D8	I/O	—	Upper byte (MSB) of data bus. This data bus is used by applications to access register files and FIFO data.
AD7:AD0	I/O	—	Lower byte (LSB) of data bus when ADSEL is LOW. Address and lower byte of data bus are multiplexed when ADSEL is HIGH.
A7:A0	I	—	Address when ADSEL is LOW. This address signal is used by application to access register files and FIFO data. This signal is ignored (all lows or all highs) when ADSEL is HIGH.
$\overline{\text{CS}}$	I	LOW	Chip Select. When this signal is asserted LOW, the ML60851A is selected and ready to read or write data.
$\overline{\text{RD}}$	I	LOW	Read Strobe. When this signal is asserted LOW, the Read instruction is executed.
$\overline{\text{WR}}$	I	LOW	Write Strobe. When this signal is asserted LOW, the Write instruction is executed.
$\overline{\text{INTR}}$	O	LOW (Note 1)	Interrupt Request. When this signal is asserted, the ML60851A makes an interrupt request to the application.
$\overline{\text{DREQ}}$	O	LOW (Note 1)	DMA Request. This signal requests the Endpoint FIFO to make a DMA transfer.
DACK	I	HIGH (Note 1)	DMA Acknowledge Signal. This signal, when asserted, enables accessing FIFOs, without address bus setting.
ALE	I	—	When ADSEL is HIGH, the address and $\overline{\text{CS}}$ on AD7:AD0 is latched at the trailing edge of this signal. This signal is ignored when ADSEL is LOW.
ADSEL	I	—	When ADSEL is LOW, the address is input on A7:A0 and data i input on D15:D8 and AD7:AD0. When ADSEL is HIGH, the lower bytes (LSB) of address and data are multiplexed on AD7:AD0.
$\overline{\text{RESET}}$	I	LOW	System Reset. When this signal is asserted LOW, the ML60851A is reset. When the ML60851A is powered on, this signal must be asserted for 1 µs.

Note: 1. Initial value immediately after resetting. Its assertion can be changed by programming.

Functional Description

The ML60851A USB device controller contains the Protocol Engine, DPLL, Timer, Status/Control, FIFO Control, Application Interface, and Remote Wakeup blocks.

- Protocol Engine
  The Protocol Engine handles the USB communication protocol. It performs control of packet transmission/reception, generation/detection of synchronous patterns, CRC generation/checking, NRZI data modulation, bit stuffing, and packet ID (PID) generation/checking.

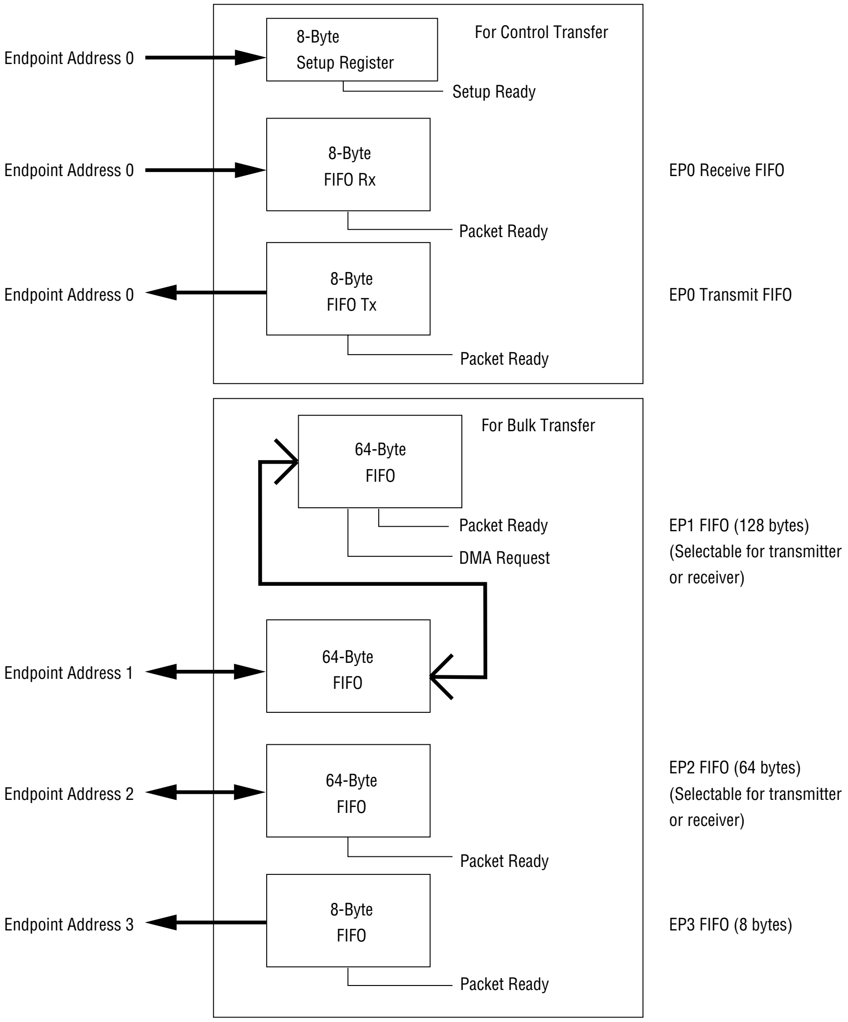
- DPLL (Digital Phase Locked Loop)
  The DPLL extracts clock and data from the USB differential received data (D+ and D–).

- Timer
  The Timer block monitors idle time on the USB bus.

- Status/Control
  The Status Control block moniors the transaction status and transmits control events to the application through an interrupt request.

- FIFO Control
  The FIFO Control block controls all FIFO operations for transmitting and receiving USB packets. The FIFO configuration is described below.

  Endpoint FIFO/8-Byte Setup Register Configuration



FIFO type	Endpoint address	Program size	Function
Reception	0	8 Bytes	Transfer control
Transmission	0	8 Bytes	Transfer control
Reception/Transmission	1	64 Bytes (2 levels)	Bulk-In and bulk-Out
Reception/Transmission	2	64 Bytes	Bulk-Out and bulk-In
Transmission	3	8 Bytes	Interrupt

Every FIFO has a flag that indicates a full or empty FIFO and the capability of re-transmitting and re-receiving data. Endpoint addresses 1 and 2 can be used for either of reception and transmission by writing the register.
The FIFO at endpoint address 1 can be used for DMA transfer.

- Interrupt
  Interrupt factors include Packet Ready for a transmit/receive FIFO, Setup Ready for 8-byte setup data, and Suspend. Generation of each interrupt request can be enabled or disabled by the Interrupt Enable register.

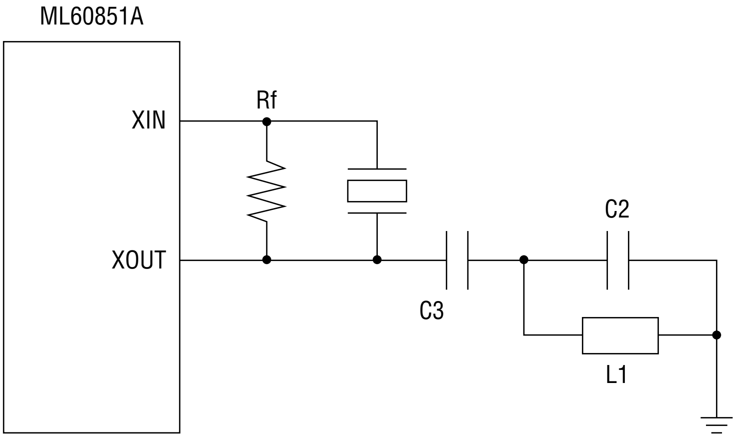
- DMA
  8-bit and 16-bit demand transfer DMA and single transfer DMA are enabled for bulk-transfer FIFO at endpoint address 1.
  In Demand Transfer mode, DREQ is asserted when a valid packet arrives at the FIFO. When the external DMA contoller has completed transferring all byte data of a received packet, DREQ is deasserted. Accordingly, other devices cannot access the local bus during DMA transfer.
  In Single Tranfer mode, each time transfer of one byte data is completed, DREQ is deasserted. While DREQ is deasserted, other devices can access the local bus.

- Remote Wakeup
  This functional block supports the remote wakeup function.

- USB Transfers
  The ML60851A supports the two transfer types (Control Transfer and Bulk Transfer) of four transfer types (Control, Isochronous, Interrupt, and Bulk) defined by the USB Specifications.
  - The Control Transfer is required for transfer of configuration, commands, and status information between the host and devices.
  - The Bulk Transfer enables transfer of a large amount of data when the bus bandwidth is enough.

- USB Transceiver
  The ML60851A contains an Oki's USB transceiver which converts internal unidirectional signals into USB-compatible signals.
  This enables the designer's application module to interface to the physical layer of the USB.

EXAMPLE OF OSCILLATOR CIRCUIT



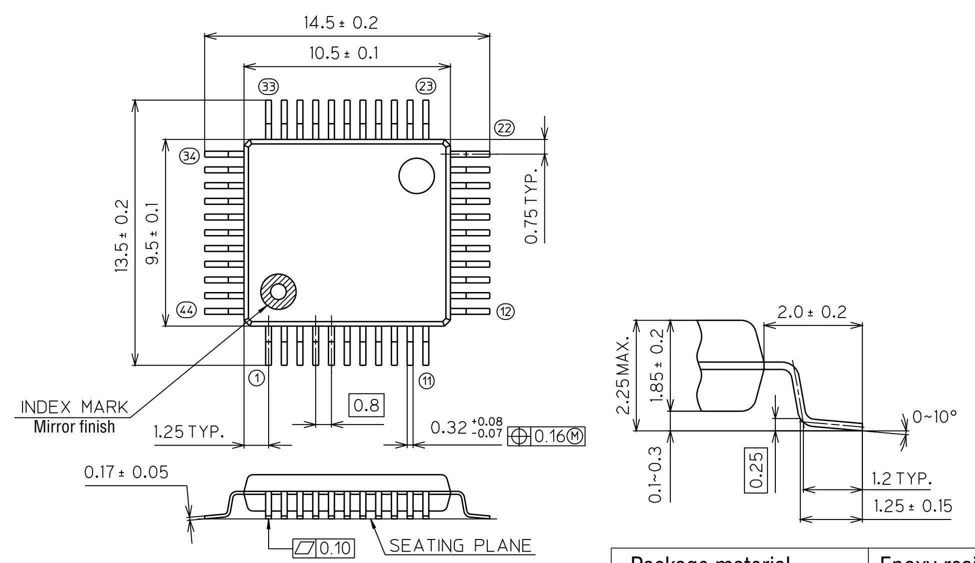
Crystal: HC-49U (KINSEKI, LTD)
C2 = 5 pF
C3 = 1000 pF
Rf = 1 MΩ
L1 = 2.2 µF

Note: The example indicated above is not guaranteed for circuit operation.

PACKAGE DIMENSIONS

(Unit : mm)

QFP44-P-910-0.80-2K



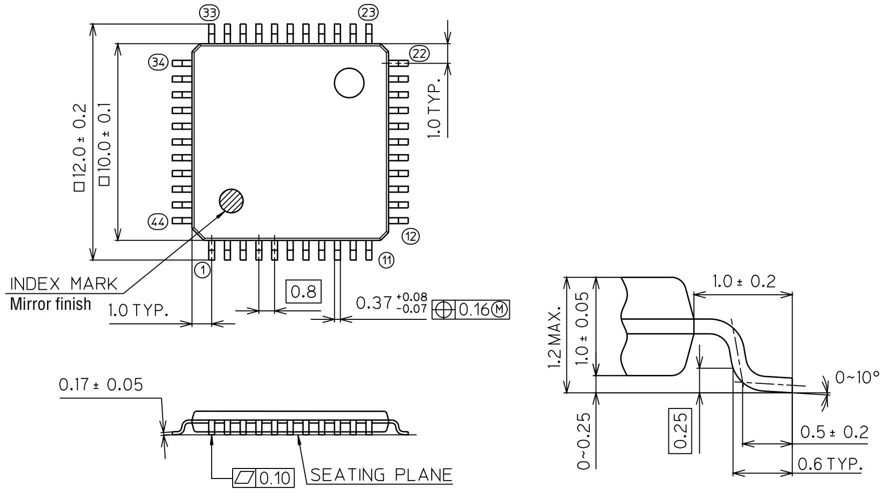
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

TQFP44-P-1010-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.28 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).