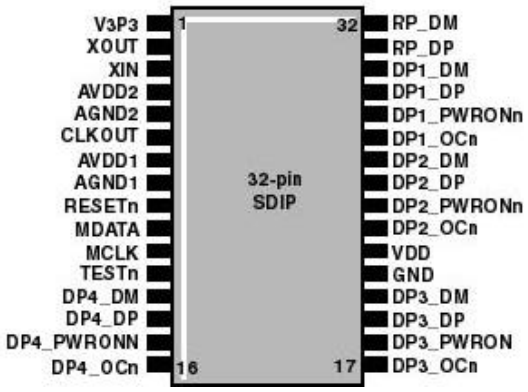
USB Monitor Hub Controller MSE9712

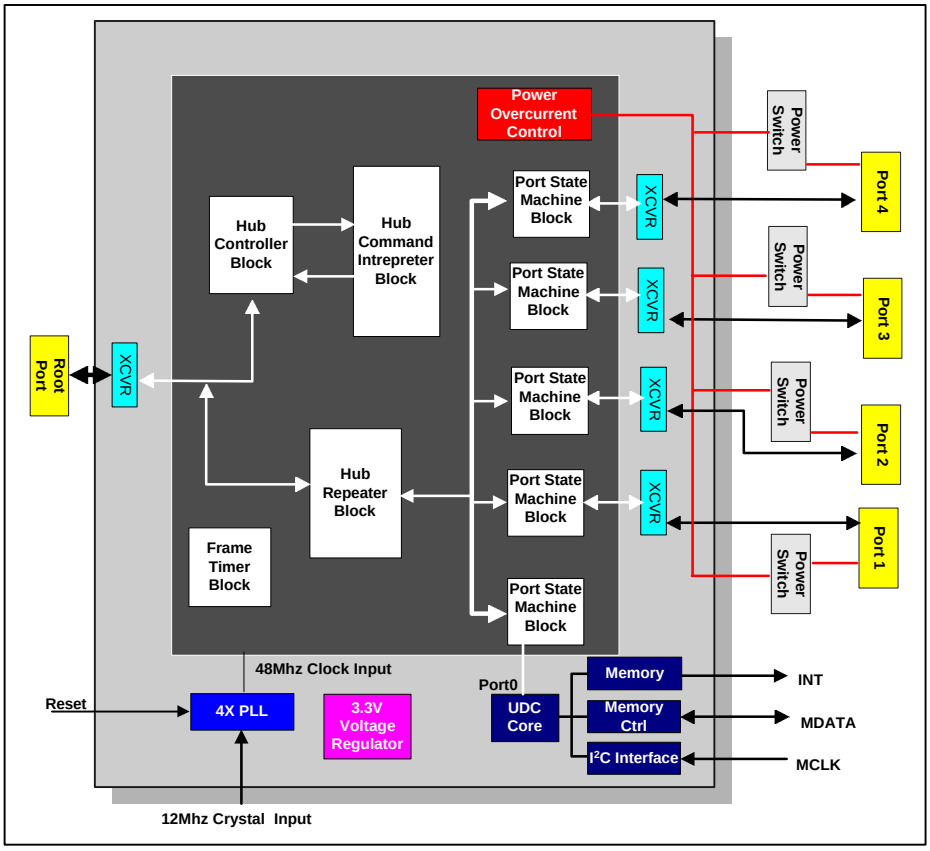
FEATURES

- Compliant with USB Protocol Revision 1.0
- No firmware required
- Four downstream ports
- Downstream device connect/disconnect detection
- Power management by supporting USB suspend/resume protocol
- Support for both low and full speed devices on the downstream ports
- Clock and data recovery from USB
- Bitstripping and Bitstuffing functions when the packets are addressed to the Hub
- CRC5 checking, CRC16 generation and checking for the packets addressed to the Hub
- Maintenance of the data toggle bits for the supported endpoints
- Output pin per port for port power switching mode and input pin per port for over-current detection
- Built-in transceivers for upstream and downstream ports
- Built-in voltage regulator
- Built-in 4X PLL clock generator
- 12Mhz clock output for external use
- I^2C compatible master/slave interface
- Compliant with USB Monitor Class Specification 1.0



DESCRIPTION

The MSE9712 is a single chip 4-port Universal Serial Bus (USB) Hub controller with I^2C compatible master/slave interface, which allows up to four USB devices and/or Hubs to connect to an upstream USB hub or USB host. The upstream USB host can send monitor class HID commands which are translated into DDC2AB commands over the I2C Bus. The MSE9712 USB Hub Controller is highly integrated requiring a minimum of external parts. The MSE9712 contains built-in transceivers, a 4X PLL clock generator with 12Mhz oscillator (requires external 12Mhz crystal), power-on reset, per-port over current detection, per-port power switching and on-board 3.3v regulator.



Pin Descriptions

Pin #	Name	I/O	Current	Type	Description
1	V3P3	PWR	-	ESD	3.3 V power output
2	XOUT	O	-	ESD	12 MHz OSC output
3	XIN	I	-	ESD	12 MHz OSC input
4	AVDD2	PWR	Double	ESD	Power for V.R. and XVER
5	AGND2	PWR	Double	ESD	Ground for V.R. and XVER
6	CLKOUT	I/O	8mA	CMOS	12 MHz or 48 MHz clock out During reset, this pin operates input pin. H : 12 MHz, L : 48 MHz
7	AVDD1	PWR	-	ESD	Analog PLL power (5 V)
8	AGND1	PWR	-	ESD	Analog PLL ground
9	RESETn	I	-	Schmit	Actually cable 5V indication input
10	MDATA	I/O	3mA	CMOS	I2C data,
11	MCLK	I/O	3mA	CMOS	I2C clock
12	TESTn	I	-	CMOS	Test mode selection H : Normal mode, L : Test mode
13	DP4_DM	I/O	-	USB	D+ for DP4
14	DP4_DP	I/O	-	USB	D- for DP4
15	DP4_PWRONn	I/O	8mA	CMOS	Power control output for DP4 During reset, this pin operates input pin. H : PLL depends on root suspend, L : PLL is always active
16	DP4_OCn	I	-	Schmit	Over current input from DP4
17	DP3_OCn	I	-	Schmit	Over current input from DP3
18	DP3_PWRONn	O	8mA	CMOS	Power control output for DP2
19	DP3_DP	I/O	-	USB	D+ for DP3
20	DP3_DM	I/O	-	USB	D- for DP3
21	GND	PWR	Double	ESD	Logic ground
22	VDD	PWR	Double	ESD	Logic power
23	DP2_OCn	I	-	Schmit	Over current input from DP2
24	DP2_PWRONn	O	8mA	CMOS	Power control output for DP2
25	DP2_DP	I/O	-	USB	D+ for DP2
26	DP2_DM	I/O	-	USB	D- for DP2
27	DP1_OCn	I	-	Schmit	Over current input from DP1
28	DP1_PWRONn	O	8mA	CMOS	Power control output for DP1
29	DP1_DP	I/O	-	USB	D+ for DP1
30	DP1_DM	I/O	-	USB	D- for DP1
31	RP_DP	I/O	-	USB	D+ for root port
32	RP_DM	I/O	-	USB	D- for root port